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September 1979

RELIABILITY EVALUATION AND ELECTRICAL CHARACTERIZATION OF MEMORIES

McDonnell-Douglas Astronautics Company

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The objective of this effort was to electrically characterize the performance of semiconductor memories implemented with different technologies and design configurations. Special emphasis was to be placed on evaluating the effectiveness of different N^2, $N^{3/2}$ and N type pattern tests to determine whether N and $N^{3/2}$ type patterns could be substituted for N^2 patterns. The results of these tests were to be incorporated into existing and proposed MIL-M-38510 specifications. The five memory types selected for characterization included: a) TMS4050, a 4K x 1 dynamic NMOS RAM, b) 93481, a 4K x 1 dynamic I^2L RAM, (Cont'd)

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c) AM9140, a 4K x 1 static NMOS RAM, d) MWS5501/CDP1821, 1K x 1 static CMOS/SOS RAMS, and e) CCD450, a 1K x 9 dynamic CCD shift register. These memories were characterized as a function of temperature, voltage and pattern sensitivity.

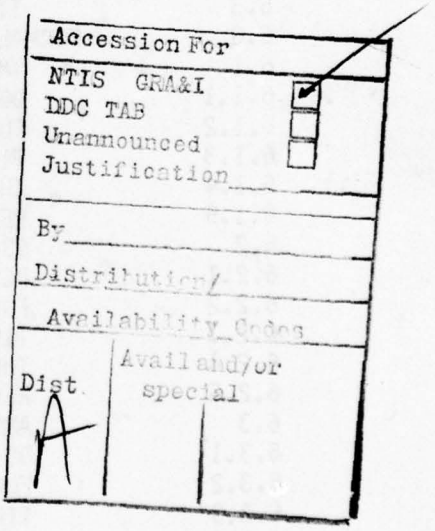
The results indicated that there were no new technology (CMOS/SOS and I^2L) related characteristics that would limit the performance of these memories. The CMOS/SOS memory was the only device to exhibit a pattern sensitivity but this is not believed to be related to the CMOS/SOS technology.

All of the static memories (NMOS and CMOS) were capable of operating over the full military temperature range (-55°C to 125°C). None of the dynamic memories (NMOS, I^2L and CCD) were capable of operating over the full military temperature range.

An analysis of pattern effectiveness suggested that N type patterns could be used in lieu of N^2 patterns for RAM electrical characterization. Except for the CMOS/SOS RAM which exhibited sensitivity to an N^2 (Walking) pattern, little difference was observed between the N and N^2 functional test results.

PREFACE

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company - St. Louis Engineering Reliability Department during the period between November 1976 and October 1978. The work was performed for the USAF Rome Air Development Center under contract Number F30602-77-C-0003. Mr. James Dobson of the RADC Solid State Applications Group provided technical direction. In addition to the many MDAC-St. Louis personnel who contributed to the program, special thanks are extended to Mr. Randy Koenig for his assistance in software development and electrical testing and to Messrs. Ron Mackin and Gordon Johnson for their many contributions to the overall test program.



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EVALUATION

The objective of this study was to establish effective reliability procedures for testing, qualifying and screening microcircuit Random Access Memories (RAMs). The study covered the performance of memories implemented with different technologies and design configurations. Special emphasis was placed on evaluating the effectiveness of various existing pattern tests, and how they can be used most effectively with each device. The purpose was to determine the optimum number and order of tests that should be done to minimize the testing required to detect pattern sensitivity.

The results of the study and discussions with the vendors were used to determine screening, testing and temperature requirements for the various RAMs. The study is considered successful in meeting the initial objectives established at the beginning of the program.

The major significance of the study is that it provides a background of technical understanding in the screening and testing of RAMs. The contractor has prepared detail specifications for MIL-M-38510, General Specification for Microcircuits, for all but two of the devices studied, using the results of the study. The study verified that the CCD450 and I2L 93481 would operate only over their specified commercial range of temperature and that no military specification for these devices should be prepared.

James J. Dobson

JAMES J. DOBSON
Project Engineer

1.0 INTRODUCTION

Complex semiconductor memory devices with storage capacities up to 4,096 bits are currently being used in Air Force systems, and memory sizes in excess of 64K bits are expected to be used in the near future. These complex devices are fabricated with a variety of different semiconductor technologies, design configurations, and test methods, all of which could introduce or conceal reliability problems. Complete electrical characterization is an essential step in assessing the reliability of these new and highly complex devices. Unfortunately, test times associated with the standard N^2 bit integrity tests (Galpat and Walking patterns) are excessive for memory sizes larger than 4K bits. More efficient test patterns are needed, and/or a different test philosophy is required.

The primary objective of the work described in this report was to electrically characterize the performance of complex memories implemented with different technologies and design configurations. Special emphasis was to be placed on evaluating the effectiveness of different N^2, $N^{3/2}$ and N type pattern tests to determine if N and $N^{3/2}$ type patterns could be substituted for N^2 patterns. Secondary objectives of the work were to formulate effective burn-in circuits for the memories and to evaluate input transient protection networks. The results of all the tests and evaluations were then to be incorporated into proposed MIL-M-38510 specifications.

2.0 MEMORY TYPES

Five different memory types were selected for characterization. These included: a) two 4096 x 1 bit dynamic random access memories, the TMS4050 which is implemented with NMOS technology, and the 93481 which is implemented with integrated injection logic (I^2L); b) one NMOS 4096 x 1 bit static RAM (AM9140); c) one CMOS/SOS 1024 x 1 bit static RAM (MWS5501/CDP1821); and d) one charge coupled 9K bit dynamic shift register (CCD450). Initially, it was hoped that the selected memories could be obtained from multiple sources. However, with one exception, devices were only available from single sources at the time characterization testing was being performed. The TMS4050 was available from several sources, but only Texas Instruments expressed an interest in supplying parts to the MIL-M-38510/235 specification. Specific manufacturers, part numbers and physical descriptions of the memories included in the program are shown in Table 2-1. Additional details of the physical and electrical characteristics of each memory type are contained in Appendices A through E.

Twenty-five devices of each memory type were obtained for electrical characterization, burn-in circuit evaluation, and transient protection network tests. A minimum of twenty of each memory type were allocated for electrical characterization. Three memories of each type were allocated for burn-in circuit evaluations, and two of each type were allocated for transient protection network tests. With the exception of the Advanced Micro Devices' (AMD) 4K static RAM (AM9140), all memories were initially obtained as commercial temperature range devices. The AMD AM9140 devices were obtained through RADC, and had been previously screened to the -55°C and 125°C electrical tests contained in the proposed MIL-M-38510/237 specification. None of the other memory types were initially available from manufacturers as full military temperature range (-55°C to 125°C) parts. However, the CDP1821, which is the microprocessor family designation for the MWS5501 CMOS/SOS static RAM, was obtained as a full military temperature range part subsequent to the MWS5501 characterization tests.

TABLE 2-1. MEMORY TYPES

PART NUMBER	TMS4050 MIL-M-38510/235	AM9140 DH9445 MIL-M-38510/237	MWS5501 CDP1821	93481	CCD450
DESCRIPTION	4Kx1 NMOS DYNAMIC RAM	4Kx1 NMOS STATIC RAM	1Kx1 CMOS/SOS STATIC RAM	4Kx1 I^2L DYNAMIC RAM	9Kx1 CCD DYNAMIC SHIFT REGISTER
MANUFACTURER	TEXAS INSTRUMENTS	ADVANCED MICRO DEVICES	RCA	FAIRCHILD	FAIRCHILD
PACKAGE TYPE	18 PIN CERAMIC DIP	22 PIN CERAMIC DIP	16 PIN CERAMIC DIP	16 PIN CERAMIC DIP	18 PIN CERAMIC DIP
LEAD MATERIALS EXTERNAL FRAME	SOLDER DIP GOLD	GOLD PLATED KOVAR GOLD	GOLD PLATED KOVAR GOLD	GOLD PLATED KOVAR GOLD	GOLD PLATED KOVAR GOLD
DIE ATTACH METALLIZATION SCRIBE	GOLD EUTECTIC ALUMINUM MECHANICAL	GOLD/SILICON EUTECTIC ALUMINUM MECHANICAL	EPOXY ALUMINUM MECHANICAL	EPOXY ALUMINUM MECHANICAL	EPOXY ALUMINUM MECHANICAL
WIRE BONDS MATERIAL CHIP FRAME	GOLD BALL ULTRASONIC	ALUMINUM ULTRASONIC ULTRASONIC	ALUMINUM ULTRASONIC ULTRASONIC	ALUMINUM ULTRASONIC ULTRASONIC	GOLD BALL ULTRASONIC
MEMORY CELL	1 TRANSISTOR CELL WITH STORAGE CAPACITOR	6 TRANSISTOR CELL	6 TRANSISTOR CELL	2 TRANSISTOR CELL WITH STORAGE CAPACITOR	1 TRANSISTOR CELL

3.0 APPROACH

Subsequent to the selection of memory types, a detailed study of individual memory characteristics was performed. This included a review of manufacturer provided functional block diagrams, logic organizations and bit maps. In some cases, manufacturers could/would not supply logic diagrams or other technical information, and the necessary information was derived from studies of the chip topology. A limited review of current literature was also performed to determine prevalent memory failure modes and electrical test problems. The results of these studies were used to establish the parameters, patterns and test conditions for preliminary electrical characterization tests. These preliminary tests were performed with two of each memory type, and were intended to provide upper and lower temperature limits, worst case supply voltage conditions, and most sensitive patterns for subsequent tests of an additional eighteen devices. Since most memory types were procured as commercial temperature range devices, it was of interest to determine performance characteristics outside of the manufacturer's specified operating temperature range. If memory performance is only slightly degraded at the -55°C and 125°C temperature limits, then characterization testing could be conducted at these temperature extremes, and full military temperature range specifications could be based on the test results. However, if the memory is not functional, or performance is degraded to the point where the part is no longer attractive for system applications, the characterization testing and specification must be accomplished at reduced temperature extremes. In some cases, only a percentage of the parts will be nonfunctional at -55°C or 125°C. Thus, judgment must be used in selecting temperature extremes, since this decision will affect the manufacturer's yield and user's cost. Maximum/minimum operating voltages, loads and combinations of these with temperature are also factors to be considered for subsequent characterization and specification.

The selection of pattern tests is critical for RAM characterization testing and specification, since the patterns generally recognized as being the most effective in detecting bit integrity and timing problems are time consuming N^2 type tests. During the initial studies of memory functional

blocks, logic organizations and chip topology, attempts were made to identify $N^{3/2}$ and N type patterns that would check for specific memory defects that were also checked by N^2 patterns. The selected N^2, $N^{3/2}$, and N type patterns were then used in all subsequent functional testing and shmoo plot evaluations. Two critical system application timing parameters (access time and write pulse width) were also selected for measurement while running each pattern. Other timing parameters were measured while running the patterns that resulted in the worst case values of access time and write pulse width.

Following the complete electrical characterization of a memory type, burn-in circuits suitable for 125°C burn-in and life testing were formulated. Both static (dc) and dynamic circuits were evaluated at ambient temperatures between 25°C and 125°C. Based on these evaluations, specific circuits were selected as MIL-M-38510 burn-circuits. Three devices were then operated in the selected circuit for 72 hours at 125°C to verify circuit suitability. A satisfactory static bias circuit was one that: a) provided maximum rated operating device voltage, b) resulted in reasonable operating currents at 125°C, and c) provided voltage stresses that would accelerate most known failure mechanisms. Generally, it is desirable to reverse bias pn junctions in bipolar devices, and provide both positive and negative polarity stresses across gate oxides in MOS devices. These conditions are usually satisfied in complex devices with most biasing configurations. A satisfactory dynamic bias circuit was one that: a) operated the memory at maximum rated operating voltage, b) maintained reasonable current levels, and c) operated the memory in a manner approximating system usage.

The final step of the memory evaluations was a test of input transient protection networks. An input pin of two of each memory type was subjected to a voltage pulse simulating a static discharge pulse (zap test). Examinations of input leakage current values prior to and following the zap test provided an indication of device damage.

4.0 INITIAL STUDY RESULTS

Two categories of memory types were included in the program, those with existing or proposed MIL-M-38510 specifications, and those with no MIL-M-38510 specification. Thus, the extent of the initial studies varied depending on the availability of a military specification. In general, if a military specification were available, sufficient studies were performed to verify the suitability and adequacy of tests contained in the specification. Additional tests were identified for characterization testing only if the MIL-M-38510 specification was clearly deficient, or if additional tests were necessary to evaluate the effectiveness of a less time consuming pattern test. Test parameters and test conditions for memories with no military specification were patterned after those contained in MIL-M-38510 specifications for devices manufactured with the same or similar technologies. In general, this was only helpful for dc parameters and loading conditions. The selections of pattern tests, timing parameters, and related voltage conditions were based on studies of current literature, manufacturer's functional diagrams, bit maps, and chip topologies. Included in the following paragraphs are discussions of the rationale employed for selection of tests and conditions related to: a) dc parameters, b) noise margins, c) quiescent power dissipation, d) bit integrity tests, e) timing parameters including refresh requirements for dynamic RAMs, and f) output loading conditions.

4.1 DC PARAMETERS

DC parameters considered for characterization included: a) input leakage currents, b) output leakage currents, c) power supply currents, d) input clamp voltages, and e) output voltages. For electrical characterization and specification it is sufficient to establish the voltage and current conditions that will yield worst case values of the parameter under test. A summary of the conditions established for dc testing is shown in Table 4-1.

MOS/CMOS input currents with both high and low level voltage inputs are primarily leakage currents, and the worst case conditions to produce maximum leakage currents are maximum supply voltage and either maximum input voltage

TABLE 4-1. WORST CASE DC TEST CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS
HIGH LEVEL INPUT CURRENT	I_{IH}	V_{CC} IS AT MAXIMUM OPERATING SUPPLY VOLTAGE INPUTS NOT UNDER TEST ARE GROUNDED V_{INPUT} UNDER TEST IS AT MAXIMUM INPUT VOLTAGE EACH INPUT IS TESTED SEPARATELY
LOW LEVEL INPUT CURRENT	I_{IL}	V_{CC} IS AT MAXIMUM OPERATING SUPPLY VOLTAGE INPUTS NOT UNDER TEST ARE AT MAXIMUM INPUT VOLTAGE V_{INPUT} UNDER TEST IS AT MINIMUM INPUT VOLTAGE EACH INPUT IS TESTED SEPARATELY
HIGH IMPEDANCE STATE, HIGH LEVEL OUTPUT CURRENT	I_{OHZ}	V_{CC} IS AT MAXIMUM OPERATING SUPPLY VOLTAGE V_{INPUTS} ARE AT MINIMUM INPUT VOLTAGES $V_{OUTPUTS}$ ARE AT MAXIMUM OUTPUT VOLTAGES CHIP IS NOT ENABLED EACH OUTPUT IS TESTED SEPARATELY
HIGH IMPEDANCE STATE, LOW LEVEL OUTPUT CURRENT	I_{OLZ}	V_{CC} IS AT MAXIMUM OPERATING SUPPLY VOLTAGE V_{INPUTS} ARE AT MINIMUM INPUT VOLTAGES $V_{OUTPUTS}$ ARE AT MINIMUM OUTPUT VOLTAGES CHIP IS NOT ENABLED EACH OUTPUT IS TESTED SEPARATELY
SUPPLY CURRENT FROM V_{CC} SUPPLY	I_{CC}	V_{CC} IS AT MAXIMUM OPERATING SUPPLY VOLTAGE V_{INPUTS} ARE AT MINIMUM INPUT VOLTAGES $V_{OUTPUTS}$ ARE AT MINIMUM OUTPUT VOLTAGES V_{CC} SUPPLY IS TESTED. SPECIAL CONDITIONS, E.G., CHIP DESELECTED AND POWER DOWN MODE
INPUT CLAMP VOLTAGE, POSITIVE	$V_{IC(POS)}$	V_{CC} IS GROUNDED AND V_{SS} IS OPEN INPUTS ARE OPEN INPUT UNDER TEST SINKS DESIRED CURRENT EACH INPUT IS TESTED SEPARATELY
INPUT CLAMP VOLTAGE, NEGATIVE	$V_{IC(NEG)}$	V_{CC} IS OPEN AND V_{SS} IS GROUNDED INPUTS ARE OPEN INPUT UNDER TEST SOURCES DESIRED CURRENT EACH INPUT IS TESTED SEPARATELY
HIGH LEVEL OUTPUT VOLTAGE	V_{OH}	V_{CC} IS AT MINIMUM OPERATING SUPPLY VOLTAGE V_{INPUTS} ARE AT NECESSARY VOLTAGE LEVELS AND TIMING TO WRITE DATA AND READ DATA OUTPUTS UNDER TEST SOURCE DESIRED CURRENT ALL OUTPUTS ARE TESTED SIMULTANEOUSLY
LOW LEVEL OUTPUT VOLTAGE	V_{OL}	V_{CC} IS AT MINIMUM OPERATING SUPPLY VOLTAGE V_{INPUTS} ARE AT NECESSARY VOLTAGE LEVELS AND TIMING TO WRITE DATA AND READ DATA OUTPUTS UNDER TEST SINK DESIRED CURRENT ALL OUTPUTS ARE TESTED SIMULTANEOUSLY

(high-level input current) or minimum input voltage (low-level input current). The same conditions are required for maximum I^2L/TTL input currents. However, the low-level input current is the input-stage emitter current, rather than a leakage current. Input leakage currents should be measured at each input pin with all other input pins connected to ground during high-level input current measurements, and to the supply voltage during low-level input current measurements.

Output leakage currents are generally only of importance for the high "Z" state of devices with tri-state outputs. Worst case conditions for high "Z" output leakages are similar to the conditions established for input leakages (maximum supply voltage and maximum or minimum output voltages).

Power supply currents are measured to assure maximum power dissipation limits are not exceeded. Application of the maximum power supply voltage will result in maximum current and power dissipation.

Tests to determine the presence of input clamp diodes require forcing a suitable current at the input pin and measuring a voltage. Network verification tests are normally not performed when the primary protection element is a field turn-on MOS transistor since proper transistor action cannot be verified via external tests. The field turn-on transistor can be verified by inducing a positive transient of several hundred volts at the device input and successfully completing the input leakage test. The TMS4050 and AM9140 NMOS memories both incorporate field turn-on transistors and the manufacturers recommended incorporating a high voltage transient test only on a sampling basis since this test is destructive. Thus, clamp diode verification tests were only used in this program for the CMOS/SOS and I^2L memories.

Output high and low voltage measurements are performed, in conjunction with input threshold measurements, to determine/verify noise margins. Minimum high level (logic "1") noise margins occur when output high voltages are minimum. Minimum low level (logic "0") noise margins occur when output low voltages are maximum. These conditions of worst case output voltage result when the supply voltage is minimum and the output loading is maximum.

4.2 NOISE MARGINS

Noise margins are defined as the difference between: a) device output low voltage (V_{OL}) and the maximum low-level input (V_{THO}) for which an output logic level does not change state, and b) device output high voltage (V_{OH}) and the minimum high-level input (V_{TH1}) for which an output does not change state. Thus, minimum noise margin is present when: a) V_{OL} is maximum and V_{THO} is minimum, and b) V_{OH} is minimum and V_{TH1} is maximum. As previously mentioned, the dc values of V_{OL} and V_{OH} are measured at conditions that result in these worst case values. Values of input voltage levels causing an output logic state change (threshold voltages - V_{TH1} and V_{THO}) should also be measured at these conditions.

4.3 POWER DISSIPATION

Maximum NMOS and I^2L device power dissipation occurs in the quiescent state with maximum power supply voltages. Thus, maximum power dissipation for these type memories can be determined from dc measurements of supply current at the various conditions of chip enable, output enable, address enable, and device power down mode. Maximum power dissipation in CMOS devices occurs during dynamic operation, and is a function of voltage, frequency and internal capacitances. Measurements of dynamic power dissipation are difficult with most automated testers since, as a minimum, the average value of supply current must be obtained over a read or write cycle period. Thus, dynamic power measurements were not included in the characterization study.

4.4 OUTPUT LOADING

The specific output loads used for each memory type during all functional and timing parameter tests are shown in Figure 4-1. These are the load configurations specified by the manufacturers, and were used to permit direct correlations between the characterization test results and the manufacturer's guaranteed performance figures.

4.5 FUNCTIONAL TESTS

RAM functional tests are performed to verify that: a) data can be stored in all memory cells, b) correct data can be retrieved from all cell locations,

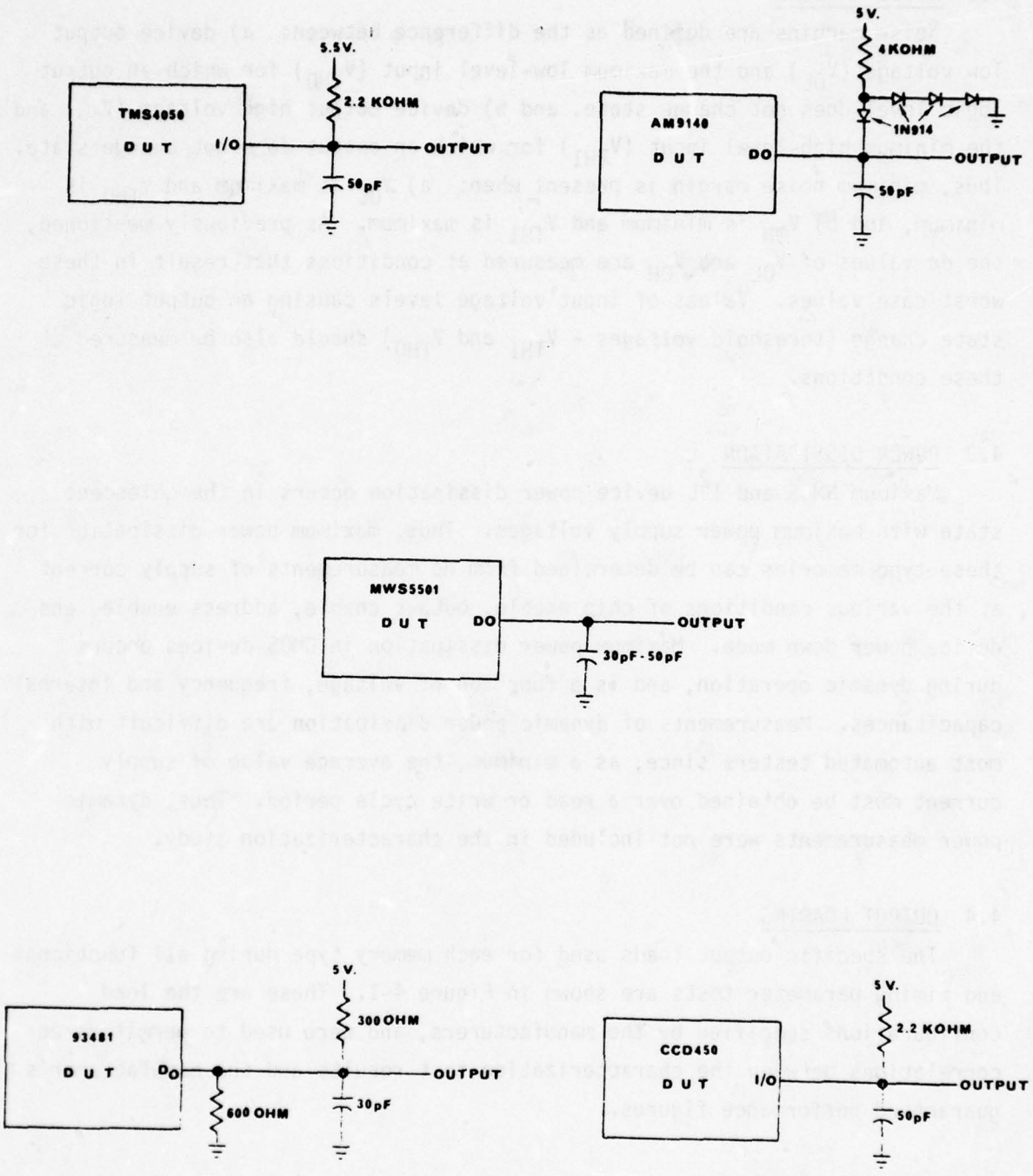


FIGURE 4-1. MEMORY DEVICE OUTPUT LOAD CIRCUITS

and c) all cells have a unique address. Memory functional tests are performed with a test pattern to show complete independence of each memory cell. Since functional tests are performed as Go/No-Go tests, a device that fails a functional test due to parameter degradation cannot be differentiated from a device that fails due to a stuck bit. For this reason, the functional tests are performed simultaneously with timing parameter measurements. The timing parameters are measured using a bisecting subroutine which utilizes a parameter value at the mid-point of a test interval with known pass/fail conditions at the interval extremes. By determining whether the device passed or failed with the mid-point value, another value is selected at the mid-point of the new pass/fail interval. The process is repeated until the interval is small enough to determine the parameter value within the desired accuracy. The two most important timing parameters, memory access time and write pulse width, were selected for measurement during functional tests, since they characterize the device during read and write operations, respectively. The definitions for these parameters are provided in Section 4.6.

Since no single pattern can exercise the memory device thoroughly enough to discover all of its deficiencies, a series of test patterns was formulated to identify specific deficiencies. The set of patterns selected was based on evaluations of device technology, functional block diagrams, logic organization, and chip topology.

4.5.1 Device Technology Review - Five process technologies are included in the memory types under evaluation: NMOS, CMOS/SOS, TTL-Schottky, I^2L and CCD. Process related defects associated with the MOS (NMOS, CMOS/SOS and CCD) technology include oxide defects, excessive leakage currents and threshold voltage shifts. For the bipolar technology (I^2L and Schottky T^2L), transistor leakage and low beta are the more common process related defects. Test patterns cannot be selected solely on the basis of device technology, since the type and location of the defect(s) will determine which pattern can detect the fault. A process related defect that causes a device functional failure due to a stuck bit at an address can be detected by a pattern which verifies all locations during read and write operations. The March (N) pattern

fulfills this requirement and is acceptable. However, other types of defects are equally likely to occur, and selection of patterns to detect these defects requires an evaluation of the functional block diagram.

4.5.2 RAM Functional Block Diagram Review - The basic RAM functional blocks include: a) address input, b) decoder, c) memory cell matrix, d) read and write amplifiers, e) clock and timing control, f) input/output (I/O), and g) special functions. Therefore, by determining which patterns will detect possible defects in each functional block, an effective set of patterns can be identified. The functional block defects may be due to inadequate design, or manufacturing process defects. Table 4-2 shows a matrix of N^2, $N^{3/2}$, and N patterns that were formulated to detect defects in each of the functional blocks. Descriptions of the pattern algorithms are included in Appendices A through D. Discussions of individual functional block defects and patterns selected to detect these defects are contained in the following paragraphs:

A) Address Input - Defects in the address input functional block typically result in an addressed cell that does not exist as an independent and unique entity. This type of failure may be caused by either a short or an open at an address input. Test patterns that read each cell at least once when each of the other cells are in a complemented state ensure that each cell has a unique address. The Galpat (N^2) pattern fulfills this requirement since all background cells are in the complemented state from the test bit cell. The test bit cell is then verified for all possible address read combinations. The sequence is repeated until each cell is used as the test bit cell. The Rowpat ($N^{3/2}$) pattern also fulfills the address uniqueness test requirement by reading the test bit cell with every other cell in its row. With the Rowpat pattern, the test bit cell is in the complemented state from the background cells. Additional test patterns that check for address uniqueness are shown in Table 4-2.

TABLE 4-2. PATTERN SELECTION BASED ON FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK	PART NUMBER	MEMORY DEFECT	PATTERN TO SCREEN WEAKNESS						
			GALPAT N^2	GALWRT N^2	WALKING N^2	ROWPAT $N^{3/2}$	MARCH N	ADDCOMP N	SHIFTING DIAGONAL N
ADDRESS INPUT	TMS4050, AM9140 MWS5501, CDP1821 AND 93481	ADDRESS UNIQUENESS	X	X	X	X	X		
DECODER		LOW SWITCHING SPEED	X	X		X		X	
		MULTIPLE ADDRESS SELECTION			X				X
MEMORY CELL		CELL DISTURB	X	X		X	X		
WRITE AMPLIFIER		SLOW WRITE RECOVERY		X			X	X	
SENSE AMPLIFIER		SLOW SENSE AMP RECOVERY			X				X
TIMING CONTROL		INACCURATE DATA	X	X	X	X	X	X	X
I/O CIRCUIT		INACCURATE DATA	X	X	X	X	X	X	X
DUMMY CELL	TMS4050	SENSE AMP IMBALANCE	X	X	X	X	X	X	X
PRECHARGE VOLTAGE GENERATOR		POOR REFERENCE VOLTAGE	X	X	X	X	X	X	X
LATCH	AM9140	INCORRECT ADDRESSING	X	X	X	X	X	X	X
LATCH	93481	INACCURATE DATA	X	X	X	X	X	X	X
FUNCTIONAL BLOCK	PART NUMBER	DEVICE DEFECT	SCAN1 N	SCAN0 N	SRWALK N	ALTWOR N	CBOARD1 N	CBOARD2 N	
SHIFT REGISTER	CCD450	CELL DISTURB			X	X	X	X	
		DATA SENSITIVITY				X	X	X	
WRITE AMPLIFIER		SLOW WRITE RECOVERY				X			
SENSE AMPLIFIER		SLOW SENSE AMP RECOVERY			X				
TIMING CONTROL		INACCURATE DATA	X	X	X	X	X	X	
I/O CIRCUIT		INACCURATE DATA	X	X	X	X	X	X	

B) Decoder - A RAM decoder failure may result in the following: (a) inaccessible memory cells, (b) memory cells with two addresses, (c) two or more memory cells with the same address, and (d) slow switching speed. Inaccessible memory cells and memory cells with two addresses can be detected by the address uniqueness patterns (Galpat, Galwrt, Walking, Rowpat and March).

Multiple cell selection is caused by a short in the address and address complement signals and can be detected by a Walking (N^2) pattern. With this pattern the background cells are written with "0s" and the test bit cell is written with a "1". The "1" is walked through every memory cell, sequentially reading all memory locations prior to shifting the test cell bit. Multiple cell selection is detected because the Walking pattern tags each memory cell with an address one at a time and shows that it shares no other address by reading the test (tag) bit as a "1" and also reading all other bits which are "0s". In addition, the Shifting Diagonal (N) pattern can detect multiple cell selection because it effectively performs a Walking pattern on separate rows. The Shifting Diagonal pattern is performed by shifting a diagonal of "1s" in a background of "0s", and the memory is read prior to shifting the diagonal. For a 64 x 64 memory cell matrix the diagonal is shifted 64 times.

Decoder switching speed is dependent on the state of the decoder prior to switching and the desired state after switching. A pattern such as Galpat that checks all possible address combinations is an effective pattern to detect this weakness. However, Galpat uses a sequential addressing scheme in performing its read combinations. A pattern that uses nonsequential addressing such as a complementary address sequence will impose a more severe test for decoder switching speed because this pattern causes more address transitions and decoder delays due to noise generation. The address complement or Addcomp (N) pattern writes the background data, reads the data in the first cell, writes its complement, increments to the maximum address, reads the data at the maximum address, and writes its complement. Following this, the second cell is read and the complement is written. The maximum address minus one (4094 for the TMS4050) is read and its complement is written. This process is

repeated until the total memory is read and its complement is written into memory.

C) Memory Cell Matrix - In addition to the previously mentioned single bit memory cell failures, the matrix may show a disturb sensitivity, i.e., data written in one cell may affect the contents of an adjacent cell. The selected cell is connected to the adjacent cell(s) by stray capacitance and can be affected by "1" to "0" and "0" to "1" transitions. Cell disturb problems can be effectively screened with a March pattern. The March pattern sequentially reads a cell and writes the complement into the cell before proceeding to the next cell. The pattern is also conducted from highest address to lowest address in the read/write sequence and then repeated with the data complemented. By performing this pattern sequence, all transitions for cell disturb are checked [1]. The Galpat pattern will also screen for cell disturb problems, but it verifies all memory cells with the test bit cell, not just adjacent bits.

D) Write/Sense Amplifier - A typical write amplifier problem associated with single I/O line memories is failure of the amplifier to recover from a write cycle in time to perform a read cycle. This write recovery delay may be due to the use of a higher voltage for the write operation than the read operation. Thus, a longer time is required to return to the normal level following a write operation. An alternate explanation is that a long recovery time may be caused by a saturated sense amplifier during a write cycle. The sense amplifier cannot recover to detect the cell voltage during a read cycle. The most effective pattern to detect both of these problems is the Galwrt (N^2) pattern. This pattern checks write-read combinations at every pair of memory cells. The Addcomp pattern is also suitable to detect write recovery problems, since every read cycle is preceded by a write cycle in a different memory cell. If the slow write recovery is due to a saturated sense amplifier, the anomalous condition can be detected by a March pattern, since write and read cycles are conducted at every memory cell.

Saturated sense amplifiers may be the result of charge accumulation at the sense amplifier input. This results in improperly identifying a "0" as a "1" after reading a long string of "1s". The Walking pattern, as described earlier, is suitable for detecting sense amplifier recovery problems, because the sense amplifier remains in the same state after reading the test bit until the test bit is "Walked" to the second location. The Shifting Diagonal pattern will also detect this weakness by writing a diagonal of "1s" in a background of "0s" and subsequently reading the memory. The single "1" in a row will be followed by a string of sixty-three (63) "0s".

E) Timing Control - The timing control functional block includes the control logic for inputs and outputs as well as the internally generated clock signals. Defects in the timing control circuitry will result in inaccurate data due to failure of the memory to write or read properly. Any pattern that can write and read data and its complement from all memory cell locations is suitable for detecting these type defects.

F) I/O Circuitry - The final functional block of every RAM is the I/O circuit, which may include a single I/O line, or separate data input and data output lines. There are no identified defects with this functional block other than inaccurate data caused by a shorted or open circuit. Any pattern that can write and read data and its complement from all memory locations is suitable.

G) Special Functions - In addition to the functional blocks included for all RAMs, the TMS4050 catalog sheet block diagram illustrates the use of dummy cells and a precharge voltage generator. The dummy cells are identical to the memory cells and minimize the sense amplifier imbalance caused by coupling noise and provide a reference voltage to the sense amplifier for discrimination of logic levels. During sense amplifier switching a proper voltage level is required, and the precharge voltage generator precharges the storage capacitor of the dummy cell to the required value [2]. A failure of either dummy cell or precharge voltage generator will provide inaccurate data at the output. These defects are easily detected by any of the previously described patterns.

The AM9140 memory includes two additional functional blocks, latch and memory status. The latch is used to isolate the address register from the address input pins, and is under clock control. In the decoder circuitry, a latch holds the select line low and prevents it from floating when all row drivers are turned off [3]. Both latches are transparent to the user and the requirement for address hold time after chip enable goes high must be satisfied. A defect in the latch circuit could result in incorrect addressing or inaccessible cells. These defects are detectable with any of the previously described patterns. The memory status is derived from internal timing signals that show the performance of a reference row of memory cells. The memory status is always enabled and never enters a three state "off" mode, and, therefore, always reflects the status of the memory. The memory status functional block is independent of the memory cell operation, and defects in this block will not affect primary memory operation.

A data latch circuit is included in the 93481. This circuit uses timing and control signals to latch output data within the timing constraints of address, address enable and latch enable signals. As long as the latch enable remains low, the output data will be latched. Inaccurate data will result with an anamolous condition in the data latch circuitry. Any pattern that reads or writes data and its complement into the memory is suitable for detecting defects in the data latch circuitry.

4.5.3 CCD Shift Register Functional Block Diagram Review - The set of patterns selected for functional testing of the CCD shift register included: Scan1 (N), Scan0 (N), Srwalk (N), Altwor (N), Cboard1 (N), and Cboard2 (N). Since the CCD450 contains no address decoder, a pattern that verifies that "1s" and "0s" can be written into and read from all memory cells should be sufficient [4]. However, a review of the functional block diagram suggested that slow sense amplifier recovery time could be a problem. Thus, a pattern similar to the Walking pattern (Srwalk) was included in the pattern set. The Srwalk pattern shifts a "1" followed by a string (1024) of "0s" through the memory, and then repeats the sequence with the data complemented.

4.5.4 Logic Organization/Schematic Review - Detailed schematics were not available from the manufacturers for all the part types. However, logic diagrams were available from the military specifications for the TMS4050 and from the manufacturer for the MWS5501/CDP1821. The TMS4050 uses clock signals in the decoding network such that the decoder outputs deselect prior to selection and inhibit possible multiple cell selections. However, the delayed clock ϕ_{DS} shown in Appendix A, Figure A3, is turned on after all signals at the decoder are stabilized. If ϕ_{DS} is turned on prematurely, multiple cell selection may occur by creating a sneak path between two storage cells. A similar condition exists for the AM9140 where several delayed clock signals are generated in the memory. A premature clock may cause the decoder to be selected and possible multiple cell selection may occur. For the MWS5501 and CDP1821 memories, slow rise or fall times may cause loss of data in the memory, or possible multiple cell selections. The MWS5501 rise and fall times must be faster than 200 nS and the newer CDP1821 rise and fall time must be faster than 1 μS.

These multiple cell selections for the TMS4050, AM9140 and MWS5501 can be detected by a Walking or Shifting Diagonal pattern as described earlier. No new patterns were added as a result of the logic diagram review.

4.5.5 Chip Topology Review - Assurance that memory cell adjacency was physically realized during functional testing was accomplished by verifying the bit map with the manufacturer, and then using the proper address sequence for physically adjacent cells. Chip topology considerations do not require new patterns, but only highlight the importance of performing functional tests with "topologically pure" patterns.

4.6 TIMING PARAMETERS

Timing parameter tests are performed to evaluate the timing relationships among the various control and address signals. Timing parameters considered for characterization included: a) access time, b) address hold time, c) address setup time, d) write pulse width, e) data hold time, and f) data setup time. These parameters are measured during a read/write cycle and/or a

read/modify/write cycle, whichever provides the worst case timing relationship for the parameter under test. A comparison of the timing parameters selected for each memory type is presented in Table 4-3.

Access time is the time after which data output is guaranteed to be valid, and may be defined with reference to either the address or chip enable signals. Access time is normally measured during a read/write cycle and read/modify/write cycle. The manufacturer's catalog specification or, when available, the military specification for the memory type, was used to select the start and stop times of the address, data, and clock signals. Since access time is a critical memory parameter, it is included in the timing tests for all part types.

Address setup time is defined as the time interval between the application of an address input and an active transition of the clock (chip enable, chip select or address enable) signals. This parameter is specified as a minimum value to ensure proper memory operation. Setup time is also specified for data input and is the time interval between the application of data and the active transition of the write pulse. The address and data setup times are specified as a minimum of 0 nS, and engineering judgment was used to exclude these tests for several part types. However, the parameters were, as a minimum, verified implicitly by adjusting the start and stop times of address, data, and clock signals and verifying that the device is functional with these timing relationships.

The write cycle requires that, in addition to the address and data timing signals, write pulse and chip enable signals occur. The "ANDED" condition of write pulse and chip enable must last for a minimum time, which is specified as write pulse width. This parameter is also measured during functional tests, but is included in the timing tests to establish the worst case values for the read/modify/write cycles. Since write pulse width is as critical a parameter as access time, it was also measured for all part types.

TABLE 4-3. COMPARISON OF TIMING PARAMETERS SELECTED

TIMING PARAMETER	TIMING PARAMETERS SELECTED				
	TMS4050	AM9140	MWS5501	93481	CCD450
ACCESS TIME	X	X	X	X	X
ADDRESS HOLD TIME	X	-	-	X	N/A
ADDRESS SETUP TIME	-	-	-	X	N/A
WRITE PULSE WIDTH	X	X	X	X	N/A
DATA HOLD TIME	X	X	X	X	X
DATA SETUP TIME	-	X	X	X	X

The address (data) hold times are defined as the interval during which the address (data) is retained after the chip enable signal goes high (low). Data hold time measurements are included for all memory types, but address hold time measurements were only included for the dynamic RAMs. Static RAM address hold times are implicitly determined during other tests.

Additional timing parameters were included for TMS4050 and AM9140 evaluations. These additional parameters included: a) propagation delay time for the TMS4050, and b) output ON/OFF delay time, memory status delay time, and preset interval time for the AM9140. The timing relationships for these signals are included in Appendices A and B.

4.7 REFRESH TESTS

Dynamic memories store data by placing a charge on a capacitor. Since the stored charge will dissipate within milliseconds, the charge must be refreshed periodically to retain correct data. Refresh requirements are temperature dependent, and at higher temperatures the refresh time will be shorter due to higher leakage currents. Refresh is accomplished in the TMS4050 and 93481 by performing a refresh cycle, or a memory read cycle at each row. Addressing a row will cause all cells in the row to be refreshed. Therefore, the TMS4050, which is organized as a 64 row x 64 column matrix, will require refreshing at 64 rows. The 93481 (32 row x 128 column matrix) will require refreshing at 32 rows.

Refresh time measurements can be accomplished by using either a block refresh or a distributed refresh technique. The block refresh technique consists of writing data in the entire memory, stopping all external clock signals for a designated time (refresh period) and reading the memory to verify its correctness. Then the data complement is written into the memory, and the procedure is repeated. The refresh time is then iterated until the boundary between a pass and fail condition is noted. This time is the required minimum refresh time for the memory under test. The main advantage of the block refresh technique is that data is verified in the absence of noise with external clock signals turned off. The main disadvantage of using this method

is that memory power dissipation/chip temperature is changing as the clock signals are turned "on" and "off". The resulting temperature dependent variations in refresh time make the block refresh technique an unacceptable test method [5].

The second method for measuring refresh time is the distributed refresh technique. This technique consists of writing data into the memory and continuously cycling the device. By sequentially reading the TMS4050 memory by its columns, every row will be refreshed every 64th cycle. Similarly, every row of the 93481 will be refreshed every 32nd cycle. The period is varied such that the time between write and read cycles is equal to the refresh time being examined. For example, the TMS4050 contains 4096 memory cells in a 64 x 64 cell matrix. To determine memory functionality with a 2 mS refresh time, the period or cycle time must equal the refresh time divided by the difference between the number of cells and the number of rows. This value was computed as 500 nS for the TMS4050. During the refresh tests, the memory is written with a checkerboard pattern (an alternating field of "1s" and "0s"), and using the distributed refresh method the refresh time is determined. After data is read out, the data complement is written into the memory and the procedure is repeated. The checkerboard pattern was selected for the refresh tests since it may show cell disturb and data sensitivity problems. A memory cell stored with a "0" may be disturbed by adjacent "1s", and vice versa.

5.0 PRELIMINARY CHARACTERIZATION TEST RESULTS

Major objectives of the preliminary characterization tests with two of each memory type were to determine the maximum and minimum operating temperatures, worst case voltage conditions, and worst case patterns for subsequent testing of eighteen devices.

5.1 OPERATING TEMPERATURE EXTREMES

The results of functional testing and shmoo plotting at ambient temperatures between -55°C and 125°C were used to determine the upper and lower temperature extremes for subsequent RAM characterization testing. However, shmoo plots of access time, write pulse width and refresh time versus supply voltage using all seven of the previously mentioned patterns provided the most insight for determining operating temperature extremes. Refresh time requirements for dynamic RAMs, and access time requirements for static RAMs were the parameters responsible for limiting operating temperatures to less than the full military temperature range. The following are brief discussions of the specific test results that led to the selection of operating temperature extremes for each memory.

5.1.1 TMS4050 NMOS Dynamic RAM - Refresh time requirements limited the TMS4050 operating temperature extremes to -55°C and 85°C. The maximum refresh time requirement specified by the manufacturer, and MIL-M-38510/235, is two milliseconds for V_{DD} values between 11.4 Vdc and 12.6 Vdc. This requirement was easily achieved at 25°C and -55°C, as were the specified requirements for all other parameters. However, as can be seen from the 85°C and 100°C shmoo plots of refresh time (t_{REF}) versus V_{DD} shown in Figure 5-1, the TMS4050 must be refreshed more frequently than every two milliseconds at 100°C with V_{DD} greater than 12 Vdc. Refresh time requirements less than two milliseconds were not determined, since this was felt to be the lower limit for most system applications. Below 12 Vdc at 100°C, the refresh time requirement changed abruptly from less than two milliseconds to approximately 50 milliseconds, and remained at 50 milliseconds down to a V_{DD} of less than 9 Vdc.

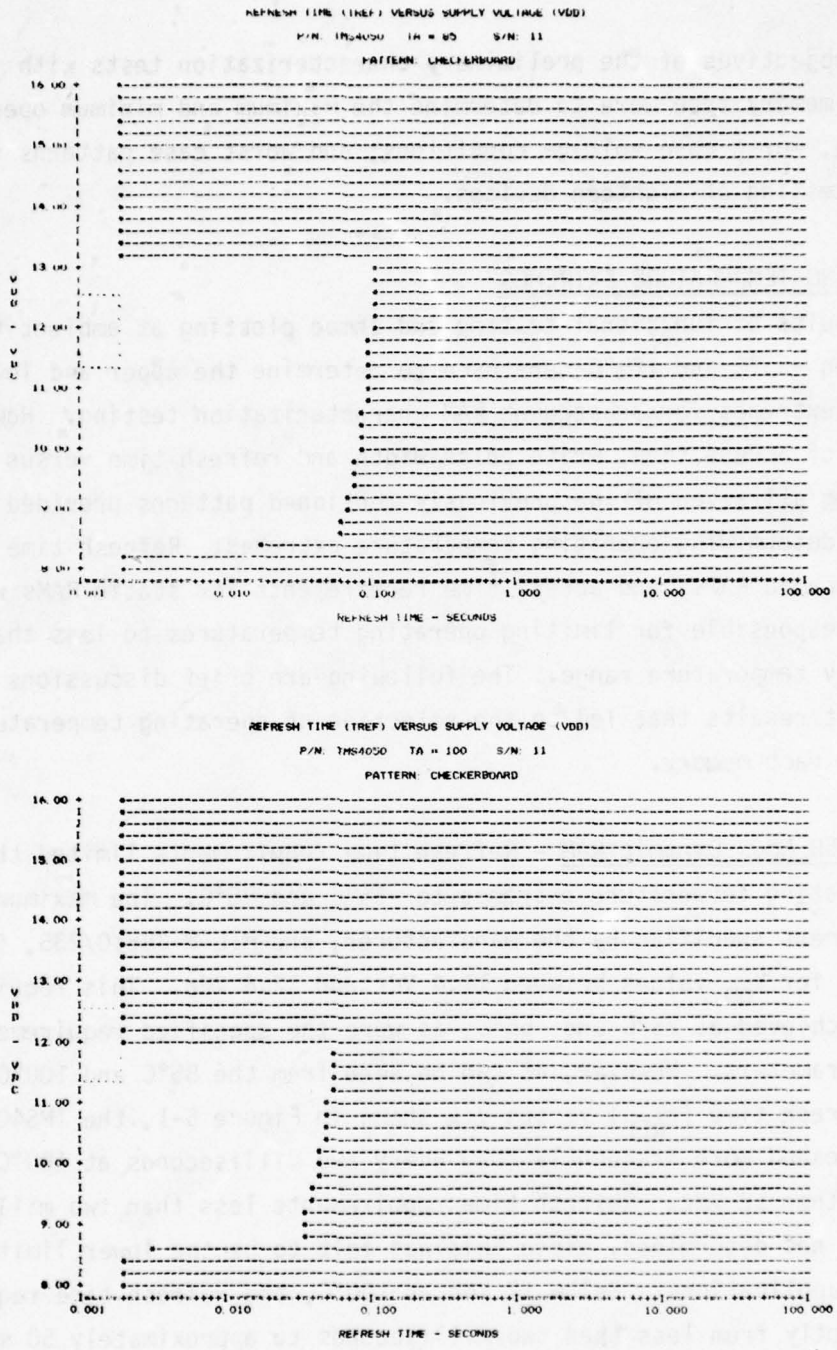


FIGURE 5-1. TEXAS INSTRUMENTS TMS4050 REFRESH TIME SHMOOS SHOWING HIGH TEMPERATURE LIMITATION

At 85°C the refresh time requirement was approximately 100 milliseconds with V_{DD} values between 8.5 Vdc and 13 Vdc. Thus, two effects were observed as the TMS4050 operating temperature was increased from 85°C to 100°C. The first effect was the expected decrease in refresh time requirement from 100 milliseconds at 85°C to 50 milliseconds at 100°C. The second, and most important, effect was the reduction in the V_{DD} value (13 Vdc at 85°C to 12 Vdc at 100°C) where the memory became nonfunctional with t_{REF} values less than two milliseconds. The second effect was the determining factor in limiting the TMS4050 upper test temperature to 85°C.

5.1.2 93481 I^2L Dynamic RAM - As was the case with the TMS4050, refresh time requirements limited the maximum temperature extremes for the 93481 I^2L dynamic RAM. However, the temperature limitations were more severe than those established for the TMS4050. The 93481 was limited to operating temperature extremes of 0°C and 70°C. Shmoo plots of t_{REF} versus V_{DD} at 70°C and 85°C are shown in Figure 5-2. At 70°C, device operation is normal with refresh times of four to five milliseconds for values of V_{DD} between 3.8 and 7 Vdc. However, at 85°C the device is only functional ($t_{REF} \geq$ two milliseconds) between 6 and 6.5 Vdc. Thus, the upper temperature limit was established as 70°C. A similar effect was noted at low temperatures, as can be seen from the 0°C and -10°C shmoo plots in Figure 5-3. At -10°C the device is not functional with values of V_{DD} less than 4.9 Vdc, and is nonfunctional at 0°C with V_{DD} values less than 4.7 Vdc. The manufacturer's lower operating limit for V_{DD} is 4.75 Vdc. Thus, 0°C was selected as the 93481 lower temperature limit. Subsequent discussions with the manufacturer revealed that the part would not operate below 0°C due to the use of four series diodes in the start-up timing circuitry. Below 0°C, the increased forward voltage of these diodes inhibits device operation. The manufacturer also noted that device operation above 70°C could be achieved, but at the expense of significant yield losses.

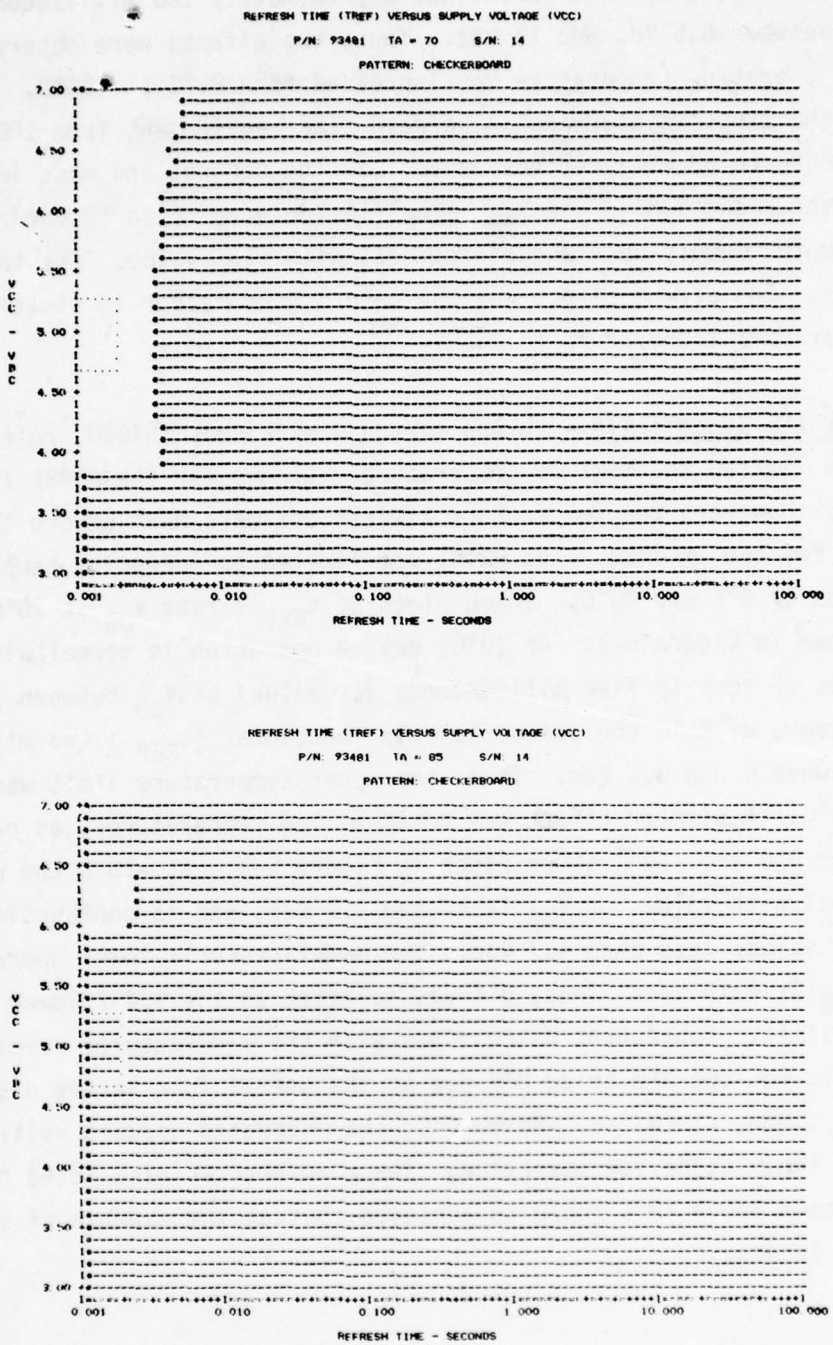
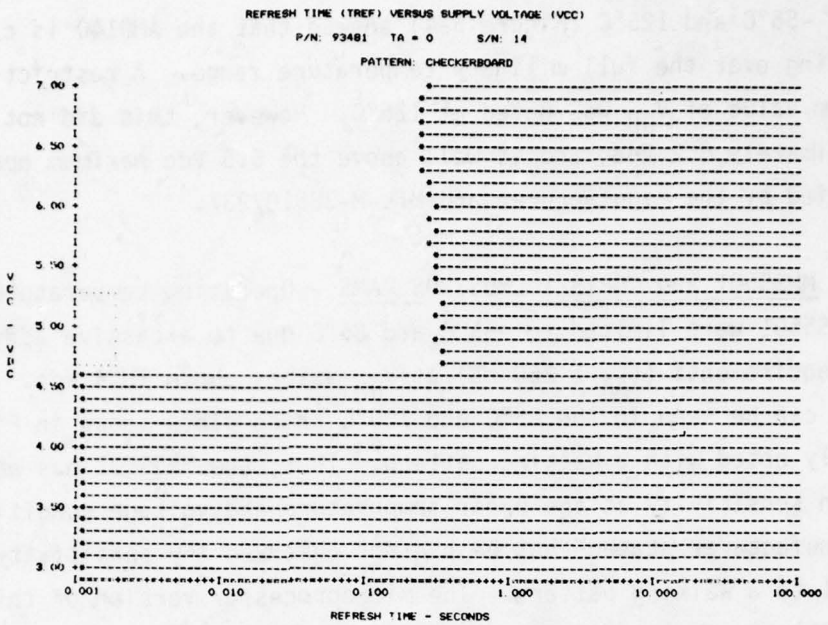


FIGURE 5-2. FAIRCHILD 93481 REFRESH TIME SHMOOS SHOWING HIGH TEMPERATURE LIMITATION



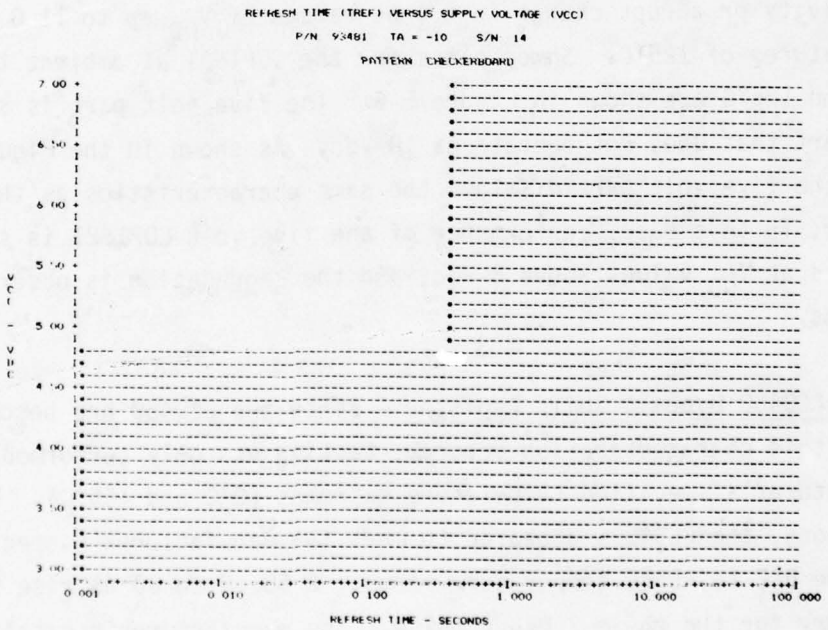


FIGURE 5-3. FAIRCHILD 93481 REFRESH TIME SHMOOS SHOWING LOW TEMPERATURE LIMITATION

5.1.3 AM9140 NMOS Static RAM - Shmoo plots of chip enable access time versus V_{DD} at -55°C and 125°C (Figure 5-4) showed that the AM9140 is capable of operating over the full military temperature range. A restriction on the maximum value of V_{DD} was noted at 125°C. However, this did not occur until approximately 6.2 Vdc, and is well above the 5.5 Vdc maximum operating voltage specified by the manufacturer and MIL-M-38510/237.

5.1.4 MWS5501 and CDP1821 CMOS/SOS RAMS - Operating temperature extremes for the MWS5501 were limited to -55°C and 85°C due to excessive address access time requirements (t_{AA} > 250 nS) at V_{DD} values above 10.4 Vdc. This effect can be seen in the 85°C and 100°C shmoo plots shown in Figure 5-5, and was only noted with a Walking pattern. Thus, the MWS5501 has an obvious pattern sensitivity at the upper temperature and voltage conditions. However, the manufacturer stated that he had not observed any sensitivity of the MWS5501 to a Walking pattern. The microprocessor version of this part (CDP1821) is supplied as either a ten volt part or a five volt part. Samples of the ten volt part provided by the manufacturer did not show any pattern sensitivity or abrupt change in t_{AA} at values of V_{DD} up to 11.0 Vdc and temperatures of 125°C. Shmoo plots for the CDP1821 at ambient temperatures of 85°C and 125°C are shown in Figure 5-6. The five volt part is simply a ten volt part that does not operate at 10 Vdc. As shown in the Figure 5-7 shmoo plot, the five volt part displays the same characteristics as the MWS5501. However, in this case, performance of the five volt CDP1821 is severly degraded at V_{DD} values above 8 Vdc, and the degradation is observed with all patterns.

5.1.5 CCD450 Dynamic Shift Register - Since the CCD450 had become obsolete during this characterization program, testing was only performed at the manufacturer's specified temperature extremes (0°C and +55°C). With two exceptions, the CCD450s appeared to meet the manufacturer's specifications over the 0°C to +55°C temperature range. A 50 nS to 60 nS rise time is mandatory for the phase 2 clock pulse. The manufacturer's catalog indicated the rise time could be as long as 200 nS, but he has subsequently confirmed the requirement for a 50 nS rise time. One of the devices tested was also sensitive to the Altwor pattern, as illustrated in Figure 5-8.

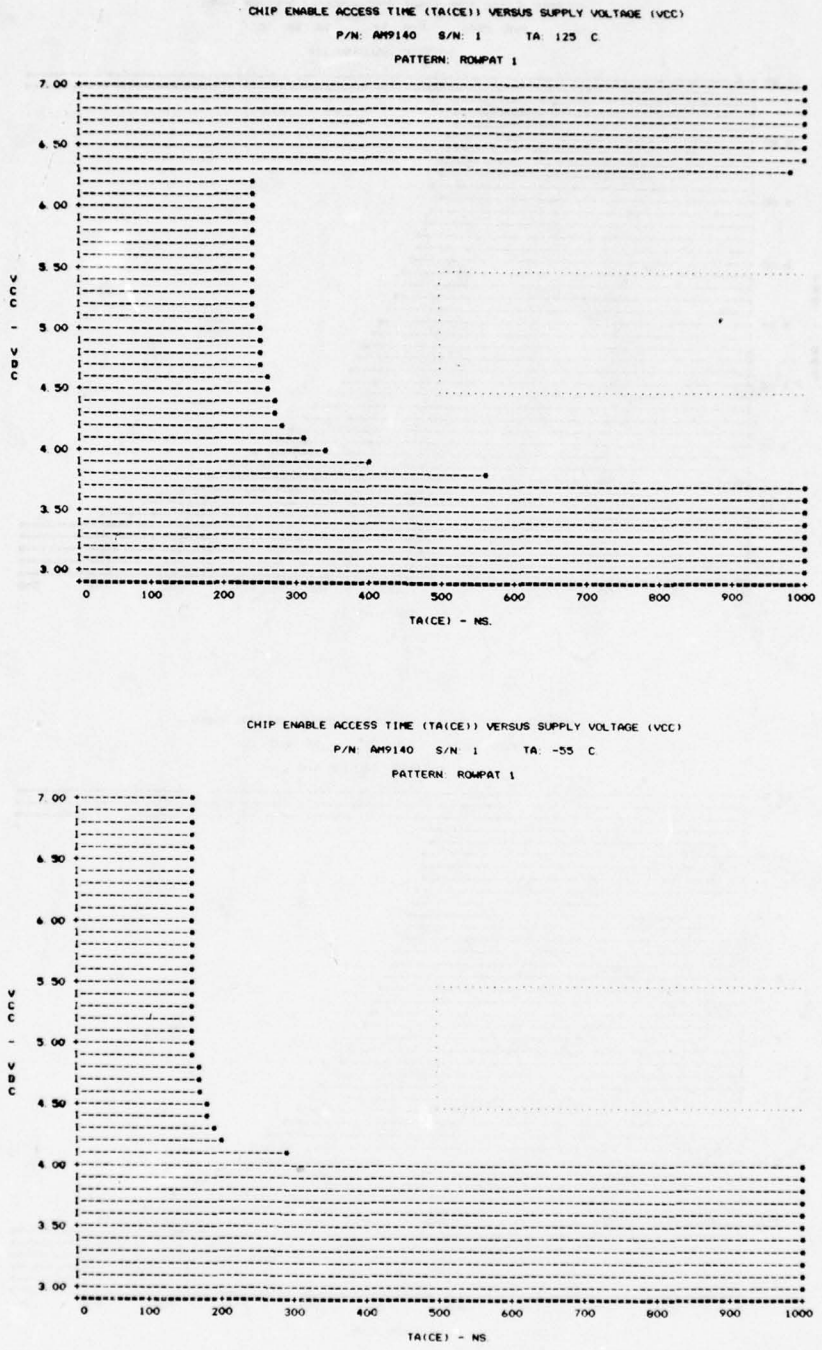
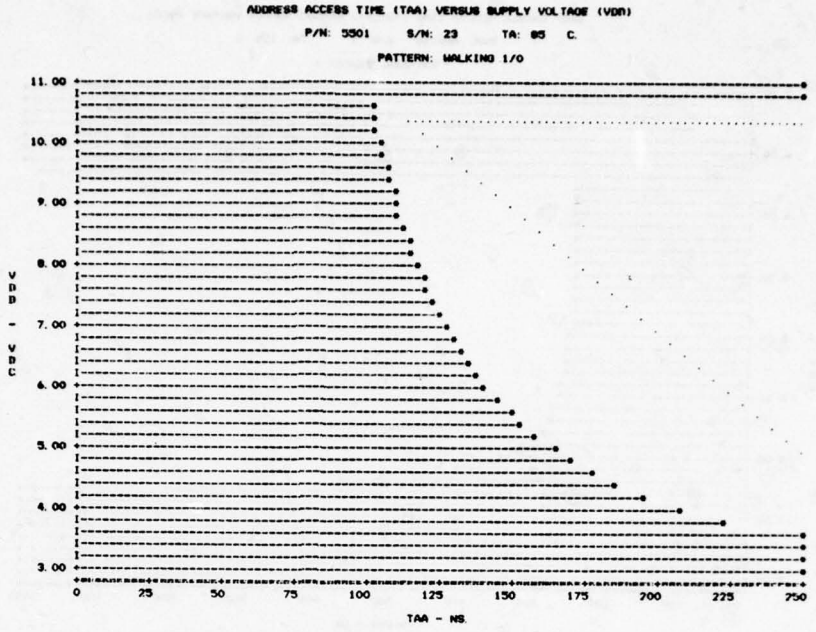


FIGURE 5-4. ADVANCED MICRO DEVICES AM9140 ACCESS TIME SHMOOS SHOWING OPERATING TEMPERATURE EXTREMES



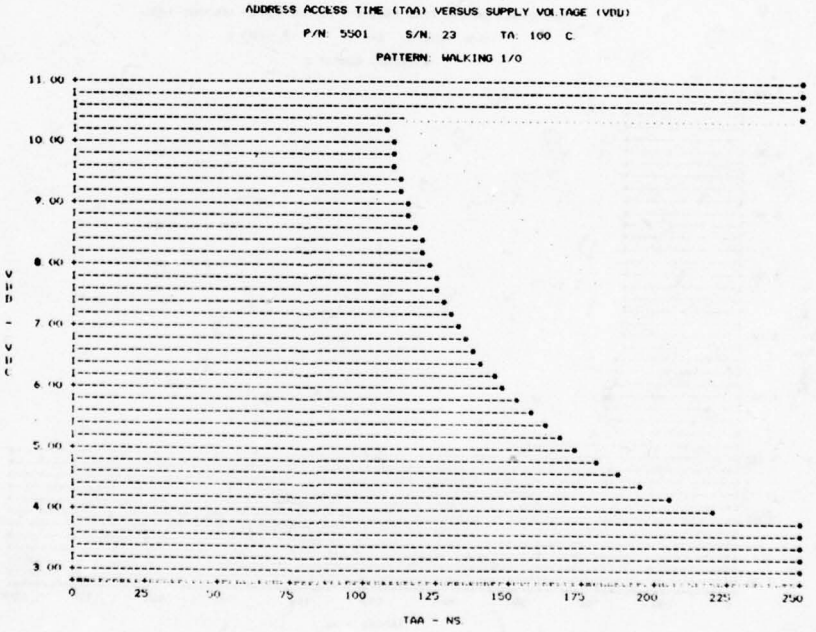
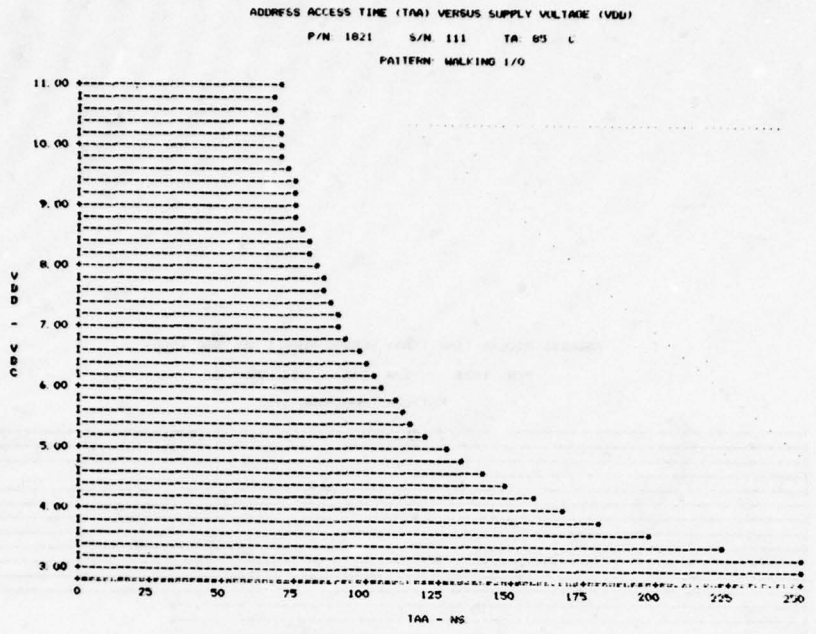


FIGURE 5-5. RCA MWS5501 ACCESS TIME SHMOOS SHOWING HIGH TEMPERATURE LIMITATION



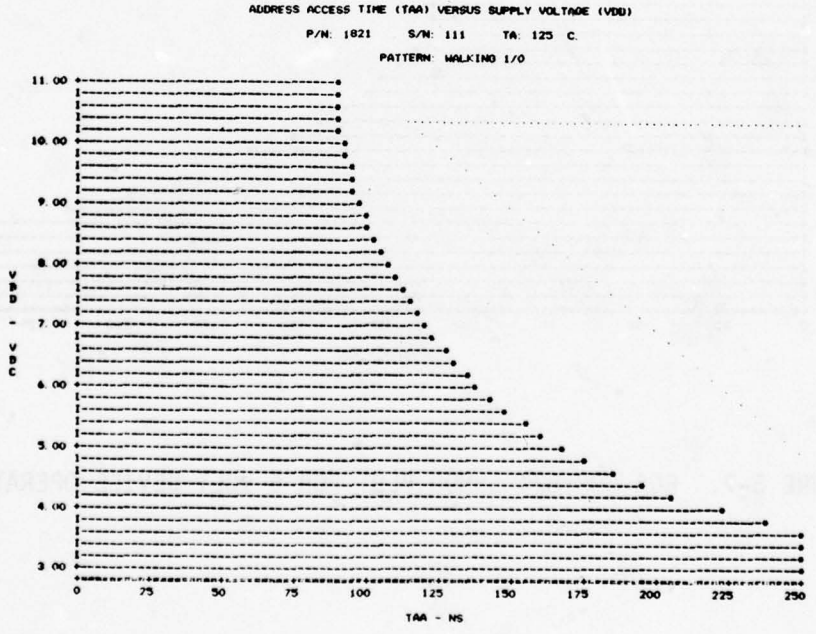


FIGURE 5-6. RCA CDP1821 ACCESS TIME SHMOOS SHOWING HIGH TEMPERATURE OPERATION

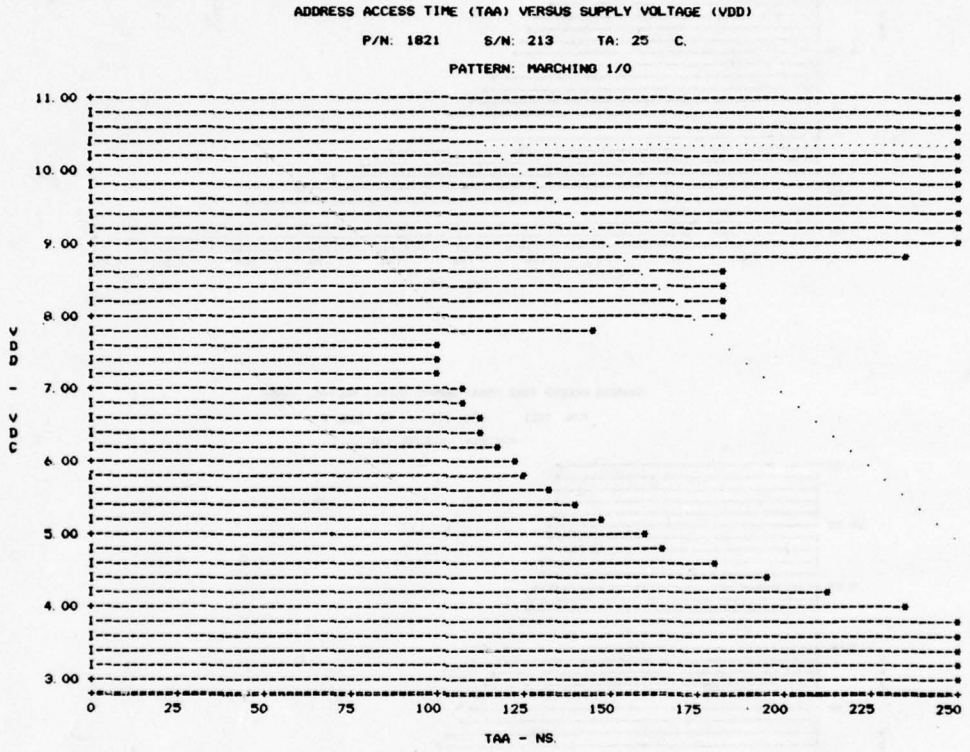
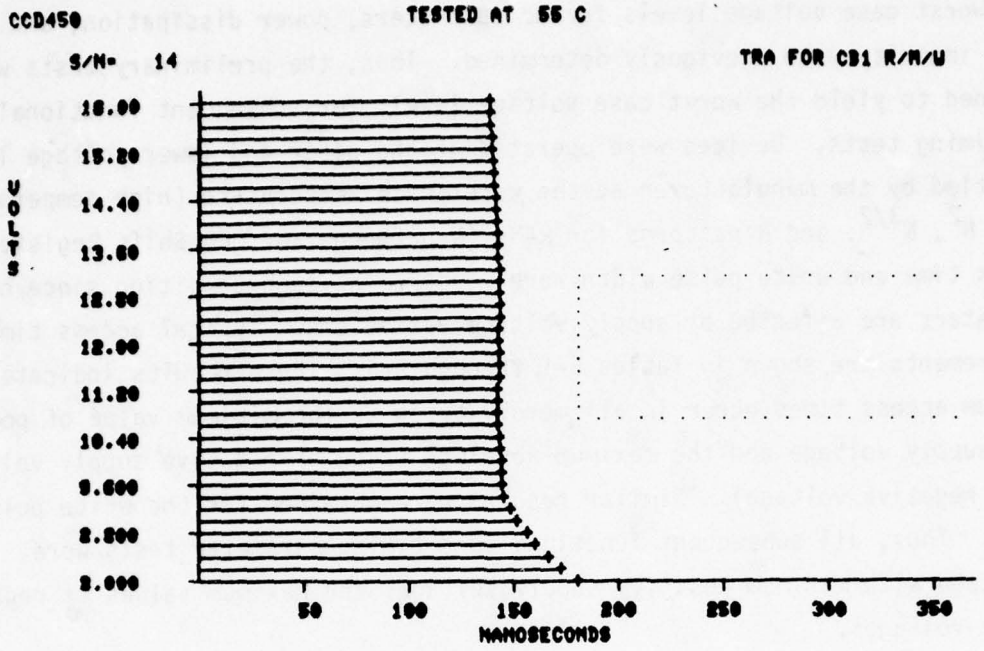


FIGURE 5-7. RCA CDP1821 SHMOO PLOT FOR 5 VOLT DEVICE OPERATION



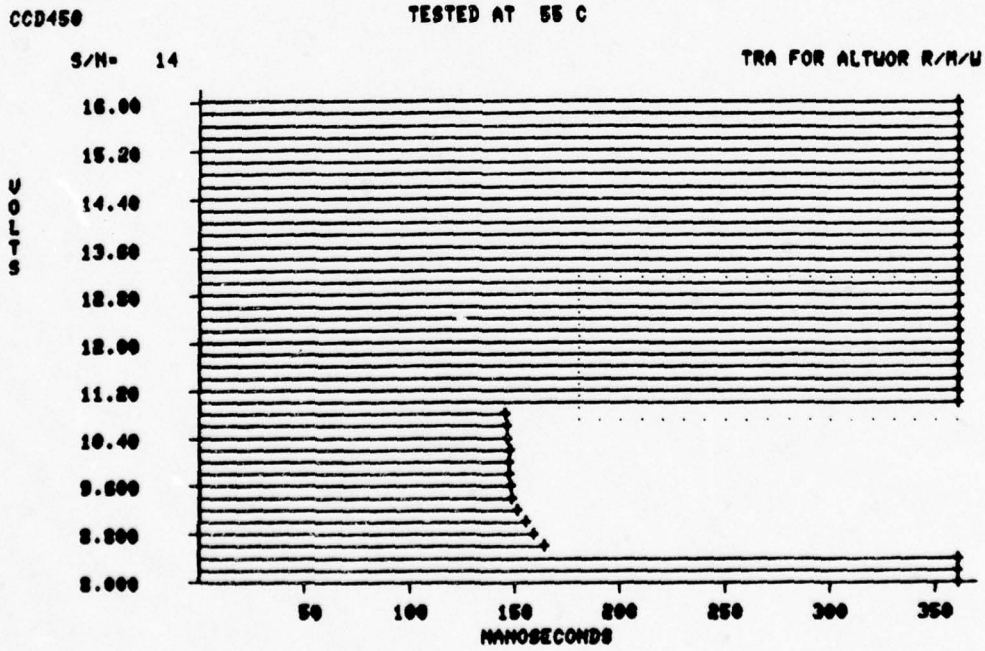


FIGURE 5-8. FAIRCHILD CCD450 ACCESS TIME SHMOOS SHOWING PATTERN SENSITIVITY AT HIGH TEMPERATURE

5.2 WORST CASE VOLTAGE LEVELS

Worst case voltage levels for dc parameters, power dissipation, and noise immunity were previously determined. Thus, the preliminary tests were designed to yield the worst case voltage levels for subsequent functional and timing tests. Devices were operated at the upper and lower voltage limits specified by the manufacturer at the worst case temperature (high temperature) using N^2, $N^{3/2}$, and N patterns for RAMs (N patterns for CCD Shift Register). Access time and write pulse width were measured at each condition since both parameters are affected by supply voltage variations. Typical access time measurements are shown in Tables 5-1 through 5-6. These results indicate that maximum access times occur in all memory types at the minimum value of positive supply voltage and the maximum absolute value of negative supply voltage (most negative voltage). Similar results were obtained for the write pulse width. Thus, all subsequent functional and timing parameter tests were conducted with minimum positive supply voltages and maximum values of negative supply voltages.

TABLE 5-1. TEXAS INSTRUMENTS TMS4050 TYPICAL ADDRESS ACCESS TIMES

PATTERN	TYPE	TYPICAL ADDRESS ACCESS TIMES				UNITS
		V_{DD} = 11.4v V_{BB} = -4.5v	V_{DD} = 11.4v V_{BB} = -5.5v ⚠1	V_{DD} = 12.6v V_{BB} = -4.5v	V_{DD} = 12.6v V_{BB} = -5.5v	
GALPAT	N^2	220	225	211	215	nS
ROWPAT	$N^{3/2}$	221	225	212	214	nS
MARCH	N	220	224	211	214	nS

NOTES:

⚠1 WORST CASE ADDRESS ACCESS TIME OCCURED AT V_{DD} = 11.4V AND V_{BB} = -5.5V.

2 MAXIMUM SPECIFICATION LIMIT FOR ADDRESS ACCESS TIME IS 300 NS.

3 AMBIENT TEMPERATURE IS 85°C.

TABLE 5-2. FAIRCHILD 93481 TYPICAL COLUMN ADDRESS TIMES

PATTERN	TYPE	TYPICAL COLUMN ADDRESS ACCESS TIMES		UNITS
		V_{CC} = 5.25v	V_{CC} = 4.75v ⚠1	
GALPAT	N^2	90	98	nS
ROWPAT	$N^{3/2}$	90	99	nS
MARCH	N	89	98	nS

NOTES:

⚠1 WORST CASE COLUMN ADDRESS ACCESS TIME OCCUR AT V_{CC} = 4.75V.

2 MAXIMUM SPECIFICATION LIMIT FOR COLUMN ADDRESS ACCESS TIME IS 75 NS.

3 AMBIENT TEMPERATURE IS 70°C.

TABLE 5-3. ADVANCED MICRO DEVICES AM9140 TYPICAL CHIP ENABLE ACCESS TIMES

PATTERN	TYPE	TYPICAL CHIP ENABLE ACCESS TIMES		UNITS
		V_{CC} = 5.5v	V_{CC} = 4.5v ⚠1	
GALPAT	N^2	244	260	nS
ROWPAT	$N^{3/2}$	246	260	nS
MARCH	N	244	257	nS

NOTES:

⚠1 WORST CASE CHIP ENABLE ACCESS TIME OCCURRED AT VCC = 4.5V.

2 MAXIMUM SPECIFICATION LIMIT FOR CHIP ENABLE ACCESS TIME IS 500 NS.

3 AMBIENT TEMPERATURE IS 125°C.

TABLE 5-4. RCA MWS5501 TYPICAL READ ACCESS TIMES

PATTERN	TYPE	TYPICAL READ ACCESS TIMES				UNITS
		V_{DD} = 10.5v	V_{DD} = 9.5v	V_{DD} = 5.25v	V_{DD} = 4.75v ⚠1	
WALKING	N^2	85	91	161	184	nS
ROWPAT	$N^{3/2}$	82	87	162	186	nS
MARCH	N	80	85	156	179	nS

NOTES:

⚠1 WORST CASE READ ACCESS TIME OCCURRED AT V_{DD} = 4.75V.

2 MAXIMUM SPECIFICATION LIMIT FOR ADDRESS ACCESS TIME IS 250 NS.

3 AMBIENT TEMPERATURE IS 85°C.

TABLE 5-5. RCA CDP1821 TYPICAL READ ACCESS TIMES

PATTERN	TYPE	TYPICAL READ ACCESS TIMES				UNITS
		V_{DD} = 10.5v	V_{DD} = 9.5v	V_{DD} = 5.25v	V_{DD} = 4.75v ⚠	
WALKING	N^2	80	83	164	183	nS
ROWPAT	$N^{3/2}$	70	73	131	145	nS
MARCH	N	72	76	132	144	nS

NOTES:

⚠ WORST CASE READ ACCESS TIME OCCURRED AT V_{DD} = 4.75V.

2 MAXIMUM SPECIFICATION LIMIT FOR ADDRESS ACCESS TIME IS 250 NS.

3 AMBIENT TEMPERATURE IS 125°C.

TABLE 5-6. FAIRCHILD CCD450 TYPICAL READ ACCESS TIMES

PATTERN	TYPE	TYPICAL READ ACCESS TIMES				UNITS
		V_{CC} = 5.25V V_{BB} = -3.00V V_{DD} = 13.20V	V_{CC} = 4.75V V_{BB} = -3.00V V_{DD} = 10.80V ⚠	V_{CC} = 4.75V V_{BB} = -2.0V V_{DD} = 13.20V	V_{CC} = 4.75V V_{BB} = -2.00V V_{DD} = 10.80V	
SRWALK	N	144	156	144	150	nS
CBOARD1	N	142	155	144	149	nS
SCAN	N	141	154	142	148	nS

NOTES:

⚠ WORST CASE READ ACCESS TIME OCCURRED AT V_{CC} = 4.75V, V_{BB} = -3.0V, AND V_{DD} = 10.80V

2 MAXIMUM SPECIFICATION LIMIT FOR READ ACCESS TIME IS 180 NS.

3 AMBIENT TEMPERATURE IS 55°C.

5.3 TIMING-TEST PATTERNS

Patterns used during the measurements of dynamic timing parameters were selected from the set of seven patterns used during functional testing. Initially, only three patterns (N^2, $N^{3/2}$, and N) were to be selected for timing parameter measurements, since these tests are extremely time consuming. Additional patterns were selected if test times were not excessive. The criteria for pattern selection was: a) select the specific N^2, $N^{3/2}$, and N pattern that yields the largest values of access time and write pulse width, and b) if no pattern related timing variations are noted, arbitrarily select at least one N^2, $N^{3/2}$, and N pattern.

The results of the RAM functional tests performed with three N^2 patterns (Galpat, Galwrt, and Walking), one $N^{3/2}$ pattern (Rowpat) and three N patterns (March, Addcomp, and Shifting Diagonal) revealed pattern related timing variations in the static RAMs (AM9140, MWS5501, and CDP1821), but none in the dynamic RAMs (TMS4050 and 93481). The average AM9140 access time values obtained with the Galwrt and Shifting Diagonal patterns were slightly lower than average values obtained with the other patterns. Thus, the Galwrt pattern was deleted for AM9140 timing parameter measurements. The Galpat pattern was also deleted, arbitrarily over the Walking pattern, but all other patterns were retained. All seven patterns were retained for MWS5501 timing parameter measurements, since test times for this 1K bit RAM were not excessive. However, the Galwrt, Addcomp, and Shifting Diagonal patterns were deleted for the subsequent tests of the CDP1821 memory to expedite the test program.

Since no pattern related timing variations were noted during functional tests of the TMS4050 and 93481 dynamic RAMs, pattern selection was arbitrary. The Galpat and Shifting Diagonal patterns were not used for TMS4050 timing parameter measurements, and the Galwrt and Walking patterns were not used for 93481 timing measurements.

Functional tests of the CCD450 shift register were performed with the following N-type patterns: Scan1, Scan0, Srwalk, Altwor, Cboard1 and Cboard2. Because of the device obsolescense, and the observed sensitivity to the Altwor pattern, only the Altwor pattern was used for timing parameter measurements.

A summary of the patterns selected for each memory type is shown in Table 5-7.

TABLE 5-7. PATTERNS USED FOR TIMING TESTS

PART TYPE	PATTERN FOR TIMING TESTS						
	GALPAT N^2	GALWRT N^2	WALKING N^2	ROWPAT $N^{3/2}$	MARCH N	ADDCOMP N	SHIFTING DIAGONAL N
TMS4050		X	X	X	X	X	
AM9140			X	X	X	X	X
MWS5501	X	X	X	X	X	X	X
CDP1821	X		X	X	X		
93481	X			X	X	X	X
PART TYPE	SCAN1 N	SCAN0 N	SRWALK N	ALTWOR N	CBOARD1 N	CBOARD2 N	
CCD450				X			

6.0 FORMAL CHARACTERIZATION TEST RESULTS

Formal characterization testing was performed with twenty of each RAM type at the temperatures and worst case voltage conditions established during the preliminary characterization tests. Only two CCD450 shift registers were formally characterized. The formal characterization tests included: a) dc parametric measurements, b) functional tests which included measurements of access time and write pulse width using N^2, $N^{3/2}$ and N patterns, c) timing parameter measurements, d) threshold voltage measurements, and e) refresh time measurements for the dynamic RAMs. Included in this section are summaries of the test results for each memory type. The summaries provide computed mean and standard deviation values for each parameter. However, parameter values outside the range of the measurement limits established by the automated test equipment have been censored from the data set. Histogram presentations of selected parameter values are provided in Appendix F.

6.1 TMS4050 TEST RESULTS

6.1.1 DC Parameters - Results of TMS4050 dc parameter tests are shown in Table 6-1. With the exception of the I_{BB} and I_{DD} (CEL) parameters, the MIL-M-38510/235 specification limits appear satisfactory. The distribution of I_{BB} values is centered well below the MIL-M-38510/235 maximum limit of 100 μA, and this limit could be reduced to 50 μA. The distribution of I_{DD} (CEL) values is well above the MIL-M-38510/234 maximum limit of 200 μA. Maximum values of I_{DD} (CEL) occured at -55°C, and the mean value at -55°C was 600 μA. The manufacturer suggested that the out-of-tolerance values of I_{DD} (CEL) were due to making the measurement before the current had reached its steady state value. As shown in Figure 6-1, there is a large I_{DD} transient when the chip enable signal goes from a high state to a low state. Thus, it is reasonable that some delay should be incorporated in the test sequence between the time the chip enable signal goes low and the I_{DD} (CEL) measurement. However, within-specification values were not realized after delays of up to 15 seconds. Thus, the MIL-M-38510/235 maximum limit for I_{DD} (CEL) probably should be increased.

TABLE 6-1. TEXAS INSTRUMENTS TMS4050 ELECTRICAL CHARACTERIZATION - DC TESTS

PARAMETER	MIL-M-38510/235 TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		±10	0.039	0.064	0.042	0.082	0.040	0.043	μAdc
I_{IL}		±10	0.024	0.004	0.028	0.004	0.029	0.002	μAdc
$I_{DD(CEH)}$		80	50.044	4.520	37.697	3.766	65.595	5.221	mAdc
$I_{DD(CEL)}$		200	352.709	192.975	211.292	170.634	599.924	285.533	μAdc
I_{BB}		-100	-5.233	2.956	-3.070	1.617	-12.088	4.272	μAdc

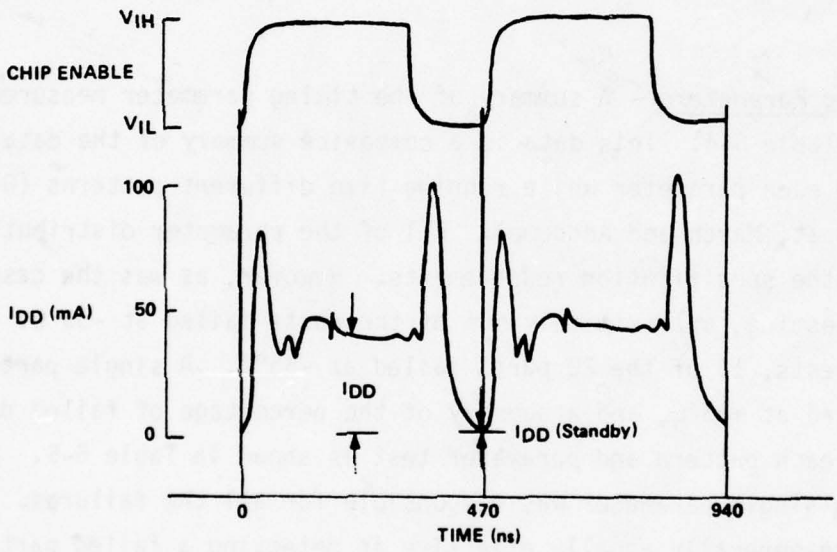


FIGURE 6-1. TEXAS INSTRUMENTS TMS4050 WAVEFORMS SHOWING STANDBY CURRENT SETTLING TIME

6.1.2 Functional Tests - The results of $t_{a(ad)}$ and $t_{w(wr)}$ measurements performed while running functional tests with the seven previously identified patterns are summarized in Table 6-2. The mean and standard deviation values reflect values within the measurement limits set for the automated test system, and show no important pattern related variations in timing parameters. At -55°C, 8 of the 20 parts tested were nonfunctional, and a summary of the percentage of these eight failures detected by each pattern is shown in Table 6-3. Note that only the Shifting Diagonal pattern detected all eight failures, suggesting that this N type pattern is the most effective pattern for detecting the observed TMS4050 functional failures. No attempt was made to analyze the nature of the failures, and the manufacturer could/would not provide additional insights.

6.1.3 Timing Parameters - A summary of the timing parameter measurements is provided in Table 6-4. This data is a composite summary of the data obtained by measuring each parameter while running five different patterns (Galwrt, Walking, Rowpat, March and Addcomp). All of the parameter distributions are well within the specification requirements. However, as was the case during functional testing, approximately 50% of the parts failed at -55°C. During the timing tests, 10 of the 20 parts failed at -55°C. A single part failure was also noted at +85°C, and a summary of the percentage of failed devices detected by each pattern and parameter test is shown in Table 6-5. Note that at -55°C, no single parameter was responsible for all the failures. All patterns were generally equally effective in detecting a failed part (all patterns detected at least 80% of the failed parts), but, the Rowpat pattern was the only pattern that was 100% effective at -55°C. Unfortunately, the single 85°C failure was not detected by Rowpat. This single failure was also not detected during functional testing although it failed a timing parameter that was measured during functional testing. The reason(s) for these apparent inconsistencies are not known, but a part intermittency could explain the observed test results.

TABLE 6-2. TEXAS INSTRUMENTS TMS4050 ELECTRICAL CHARACTERIZATION - FUNCTIONAL TESTS

PARAMETER	MIL-M-38510/235 TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
$t_{a(ad)}$		300							
GALPAT		↑	191.150	25.372	217.100	30.435	151.250	9.371	nS
GALWRT		↕	192.200	25.616	217.750	30.551	151.000	9.564	↕
WALKING		↕	192.150	25.596	217.800	30.452	150.750	9.592	↕
ROWPAT		↕	191.300	25.047	216.800	29.969	150.167	9.307	↕
MARCH		↕	190.800	25.540	216.500	30.391	149.833	9.398	↕
ADDCOMP		↕	190.000	24.893	215.500	29.803	149.000	8.642	↕
SHIFTING DIAGONAL		300	189.850	25.489	215.550	30.294	149.083	9.331	nS
$t_{w(wr)}$	200								
GALPAT	↑		27.200	4.226	33.250	5.620	20.167	1.572	nS
GALWRT	↕		27.000	4.135	33.100	5.726	20.083	1.553	↕
WALKING	↕		27.300	4.224	33.400	5.687	20.250	1.738	↕
ROWPAT	↕		27.000	4.159	33.150	5.730	20.000	1.780	↕
MARCH	↕		27.000	4.171	32.806	5.591	19.917	2.019	↕
ADDCOMP	↕		25.350	3.745	31.950	5.249	18.667	2.134	↕
SHIFTING DIAGONAL	200		26.400	4.042	32.600	5.526	19.667	2.095	nS

V_{DD} = 11.4 Vdc AND V_{BB} = -5.5 Vdc

TABLE 6-3. TEXAS INSTRUMENTS TMS4050 PATTERN EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PATTERN T_A = -55°C						
		GP	GW	W	R	M	A	SD
READ/WRITE								
$t_{a(ad)}$	>500	88	75	88	75	88	75	100
$t_{w(wr)}$	<460	88	75	88	75	88	75	100
NUMBER OF DEVICE FAILURES AT T_A		8						

NOTES:

1. GP - GALPAT
   GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL

2. NO FAILURES AT T_A = 25°C and T_A = 85°C.

3. WORST CASE SUPPLY VOLTAGES: V_{DD} = 11.4V and V_{BB} = -5.5V.

TABLE 6-4. TEXAS INSTRUMENTS TMS4050 ELECTRICAL CHARACTERIZATION - DYNAMIC TIMING TESTS

PARAMETER/ PATTERN	MIL-M-38510/235 TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
$t_{h(ad)}$	150		24.630	3.158	25.916	3.664	23.380	2.235	nS
t_{PLH}	40		177.580	20.361	162.674	65.681	64.540	1.040	nS
$t_{h(da)}$	40		18.450	2.304	16.968	2.552	17.380	1.573	nS
READ/MODIFY/WRITE									
$t_{a(ad)}$		300	172.980	26.117	197.505	31.580	134.760	3.984	nS
$t_{h(da)}$	150		19.270	2.078	18.095	2.304	18.000	1.523	nS
$t_{w(wr)}$	200		26.550	3.819	29.853	3.855	20.340	1.380	nS

V_{DD} = 11.4 Vdc AND V_{BB} = -5.5 Vdc

TABLE 6-5. TEXAS INSTRUMENTS TMS4050 DYNAMIC TIMING EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PARAMETER AND PATTERN									
		T_A = 85°C					T_A = -55°C				
		GW	W	R	M	A	GW	W	R	M	A
READ/WRITE											
$t_{h(ad)}$	<200		100		100	100	60	60	50	50	50
t_{PLH}	<360		100		100	100	40	50	50	50	50
$t_{h(da)}$	<73		100		100	100	80	90	80	80	80
READ/MODIFY/WRITE											
$t_{a(ad)}$	>470		100		100	100	50	60	60	60	50
$t_{h(da)}$	<170		100		100	100	40	50	50	50	50
$t_{w(wr)}$	<290		100		100	100	50	60	60	60	50
PERCENT FAILED DEVICES DETECTED BY PATTERN			100		100	100	90	90	100	90	80
NUMBER OF FAILED DEVICES AT T_A				1					10		

NOTES:

1. GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
2. NO FAILURES AT T_A = 25°C
3. WORST CASE SUPPLY VOLTAGE: V_{DD} = 11.4V and V_{BB} = -5.5V

6.1.4 Threshold Tests - Results of the threshold voltage tests are summarized in Table 6-6. These results affect device noise immunity, and are discussed in paragraph 9.2.

6.1.5 Refresh Tests - Refresh test results are summarized in Table 6-7. As expected, the minimum refresh time requirement occurs at the high temperature condition (85°C). The standard deviation of the distribution is also quite large, indicating a wide spread of values for this parameter. Examination of the histograms of refresh time at 85°C (Appendix F) shows a range of values from near 0 milliseconds to 130 milliseconds, but most parts are between 0 and 30 milliseconds. Only a few parts have 85°C refresh times in the 100 millisecond region.

TABLE 6-6. TEXAS INSTRUMENTS TMS4050 ELECTRICAL CHARACTERIZATION - THRESHOLD TESTS

PARAMETER	MIL-M-38510/235 TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{TH1}	-	-	1.753	0.173	1.642	0.131	1.686	0.135	Vdc
V_{THO}	-	-	0.975	0.191	0.930	0.193	0.990	0.198	Vdc

V_{DD} = 11.4 Vdc AND V_{BB} = -5.5 Vdc

TABLE 6-7. TEXAS INSTRUMENTS TMS4050 ELECTRICAL CHARACTERIZATION - REFRESH TESTS

PARAMETER	MIL-M-38510/235 TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
t_{REF} V_{DD} = 11.4v V_{BB} = 4.5v	-	2	342.419	114.378	25.241	24.519	401.094	0.791	mS
t_{REF} V_{DD} = 11.4v V_{BB} = -5.5v	-	2	323.193	113.046	23.702	23.210	401.094	0.791	mS

6.2 93481 TEST RESULTS

6.2.1 DC Parameters - The 93481 dc parameter test results are shown in Table 6-8. All of the measured parameters are well within the manufacturer's catalog limits, and tightened limits could be incorporated in a MIL-M-38510 specification. Limits are also required for the I_{CC} parameters, since the manufacturer does not specify limits for I_{CC}.

6.2.2 Functional Tests - The results of t_{CAA} and t_W measurements performed while running functional tests with seven patterns are shown in Table 6-9. No important pattern related variations in timing parameters were noted, but 7 of the 20 parts tested were not functional (6 at 0°C and 1 at 70°C). With the exception of the single failure at 70°C, all failures (Table 6-10) were detected by all patterns. The 70°C part failure was not detected by the Addcomp and Shifting Diagonal patterns. A cell-disturb type failure could produce the observed pattern sensitive results.

6.2.3 Timing Parameters - A summary of the 93481 timing parameter measurements is shown in Table 6-11. Examination of the mean and standard deviation values for each parameter shows that a high percentage of parts do not meet the manufacturer's specifications for t_{CAA} and t_W, especially at 70°C. However, only one part was not functional at 70°C, suggesting that the manufacturer's specification for t_{CAA} and t_W should be relaxed. As shown in Table 6-12, nine parts were not functional at 0°C. This high percentage (45%) is not unexpected in view of the design limitation previously discussed. It is interesting to note, however, that no single pattern was 100% effective in detecting these nine low temperature failures, nor was any single parameter responsible for all the failures. Parts that are totally nonfunctional at 0°C should have been detected by all patterns, and failed all parameter specifications. Thus, some of the 0°C failures were probably still functional parts.

TABLE 6-8. FAIRCHILD 93481 ELECTRICAL CHARACTERIZATION - DC TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 70°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		1.0	0.002	0.006	0.002	0.005	0.003	0.007	mAdc
I_{IL}		-400	-66.663	11.827	-55.021	9.691	-76.426	13.820	μAdc
I_{OH2}		100	2.396	3.841	9.131	7.549	2.203	5.305	μAdc
I_{OL2}		50	1.741	1.941	8.651	7.119	1.432	4.639	μAdc
I_{CC1}	-	-	15.775	1.643	15.407	1.730	15.928	1.782	mAdc
I_{CC2}	-	-	82.133	6.419	80.123	6.082	82.037	7.716	mAdc
I_{CC3}	-	-	8.965	0.854	8.100	0.763	9.675	1.001	mAdc
$V_{IC(NEG)}$	-	-1.5	-1.034	0.074	-0.991	0.079	-1.063	0.073	Vdc

TABLE 6-9. FAIRCHILD 93481 ELECTRICAL CHARACTERIZATION - FUNCTIONAL TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 70°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_{CAA}		75							
GALPAT		↑	76.478	4.159	82.591	3.906	75.706	6.488	nS
GALWRT		↕	75.739	3.847	81.227	3.248	74.353	6.799	↕
WALKING		↕	75.957	3.972	81.182	3.589	75.118	6.685	↕
ROWPAT		↕	75.826	4.177	80.727	3.658	74.882	7.283	↕
MARCH		↕	75.391	4.459	79.955	3.496	75.353	7.867	↕
ADDCOMP		↕	75.217	5.191	78.773	4.815	75.294	6.788	↕
SHIFTING		75	74.435	6.921	79.136	3.389	76.059	7.344	nS
DIAGONAL									
t_W	25								
GALPAT	↑		20.000	0.000	20.864	2.201	20.059	0.236	nS
GALWRT	↕		20.000	0.000	21.227	2.467	20.059	0.236	↕
WALKING	↕		20.043	0.206	22.545	4.469	20.059	0.236	↕
ROWPAT	↕		20.000	0.000	22.591	4.726	20.059	0.236	↕
MARCH	↕		19.565	0.771	20.909	2.859	19.176	1.823	↕
ADDCOMP	↕		17.217	2.766	20.182	4.821	16.706	2.136	↕
SHIFTING	25		19.739	0.674	22.091	4.199	19.941	1.211	nS
DIAGONAL									

V_{CC} = 4.75 Vdc

TABLE 6-10. FAIRCHILD 93481 PATTERN EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PATTERN													
		T_A = 70°C							T_A = 0°C						
		GP	GW	W	R	M	A	SD	GP	GW	W	R	M	A	SD
READ/WRITE															
t_{CAA}	>200	100	100	100	100	100			100	100	100	100	100	100	100
t_W	<50	100	100	100	100	100			100	100	100	100	100	100	100
NUMBER OF DEVICE FAILURES AT T_A					1							6			

NOTES:

1. GP - GALPAT
   GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL

2. NO FAILURES AT T_A = 25°C

3. WORST CASE SUPPLY VOLTAGE V_{CC} = 4.75V

TABLE 6-11. FAIRCHILD 93481 ELECTRICAL CHARACTERIZATION - DYNAMIC TIMING TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 70°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_{AS}	0		0 000	0.000	0.273	0.924	0. 071	0.593	nS
t_{AH}	45		29.904	3.118	26.145	2.508	39.314	3.639	nS
t_{WSDE}	45		19.791	6.001	24.673	8.071	18.571	4.364	nS
t_{WHD}	35		9.757	2.528	10.291	2.868	9.329	2.761	nS
READ/MODIFY/WRITE									
t_{CAA}		75	69.052	6.237	73.191	4.846	68.957	8.052	nS
t_W	25		17.783	3.567	20.973	5.096	15.429	2.638	nS
t_{CSA}		40	35.113	1.662	35.364	1.373	38.914	2.902	nS

V_{CC} = 4.75 Vdc

TABLE 6-12. FAIRCHILD 93481 DYNAMIC TIMING EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PARAMETER AND PATTERN									
		T_A = 70°C					T_A = 0°C				
		GP	R	M	A	SD	GP	R	M	A	SD
READ/WRITE											
t_{AS}	< 9						78	78	78	78	56
t_{AH}	< 59						67	78	78	78	56
t_{WSDE}	<120	100	100				78	67	78	67	67
t_{WHD}	< 35						44	44	44	44	56
READ/MODIFY/WRITE											
t_{CAA}	>200						56	56	56	56	56
t_W	< 50						56	56	56	56	56
t_{CSA}	> 80						56	56	56	56	56
PERCENT OF FAILED DEVICES DETECTED BY PATTERN		100	100				89	89	89	78	67
NUMBER OF FAILED DEVICES AT T_A		1					9				

NOTES:

1. GP - GALPAT
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL
2. NO FAILURES AT T_A = 25°C
3. WORST CASE SUPPLY VOLTAGE: V_{CC} = 4.5V

Discussions with the manufacturer about the inability of these parts to meet his catalog specifications revealed that he has redesigned the part using smaller element geometries. He stated that the new parts should meet the catalog specifications, especially the 75 nS access time requirement. However, he has no current plans to design a part capable of operation at -55°C.

6.2.4 Threshold Tests - Threshold voltage test results are summarized in Table 6-13, and are discussed in paragraph 9.2.

6.2.5 Refresh Tests - Refresh time test results are summarized in Table 6-14. As was the case with the TMS4050, there is wide spread in the distribution of parameter values, suggesting that the processes affecting this parameter are not well controlled.

TABLE 6-13. FAIRCHILD 93481 ELECTRICAL CHARACTERIZATION - THRESHOLD TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 70°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{TH1}	-	-	1.879	0.046	1.671	0.035	2.100	0.108	Vdc
V_{TH0}	-	-	1.146	0.113	1.018	0.060	1.299	0.041	Vdc

V_{CC} = 4.75 Vdc

TABLE 6-14. FAIRCHILD 93481 ELECTRICAL CHARACTERIZATION - REFRESH TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 70°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
t_{REF} V_{CC} = 4.75v	-	2	147.120	143.715	43.617	81.274	271.213	151.089	mS
t_{REF} V_{CC} = 5.25v	-	2	187.173	139.990	46.510	89.908	340.336	94.926	mS

6.3 AM9140 TEST RESULTS

6.3.1 DC Parameters - The AM9140 dc parameter test results are shown in Table 6-15. All of the measured parameter values are well within the limits contained in MIL-M-38510/237, and the limits for I_{CC} could be tightened. Electrical tests of a 120 piece lot of AM9140s for another RADC program (Contract No. F30602-78-C-0014) confirmed that the maximum values specified for I_{CC} could be reduced with no increase in yield loss.

6.3.2 Functional Tests - The results of t_A and t_W measurements performed while running functional tests with seven patterns are shown in Table 6-16. Examination of the mean values of access time obtained with each pattern shows no important pattern related variations for five of the seven patterns. However, the mean values of t_A obtained while running the Galwrt and Shifting Diagonal patterns are respectively 5% and 15% lower than the mean values of t_A obtained with the other five patterns. Without specific knowledge of where the access time variations are occurring on the chip, it is difficult to speculate why the Galwrt and Shifting Diagonal patterns yield lower access times than the other patterns.

Two of the AM9140 memories were nonfunctional at -55°C and 125°C, and as shown in Table 6-17, neither of the failures was detected with the Shifting Diagonal pattern. All failures were detected by the Galpat, Galwrt, Walking and March patterns.

6.3.3 Timing Parameters - A summary of the AM9140 timing parameter measurements is provided in Table 6-18. All of the timing parameter distributions are well within the MIL-M-38510/237 limits, and the limits for output off delay (t_{CF}) and data setup time (t_{DS}) could be more stringent if desired. Three timing parameter failures were noted at 125°C, and as shown in Table 6-19, all were detected by all patterns except the Shifting Diagonal.

6.3.4 Threshold Tests - Results of the threshold voltage tests are summarized in Table 6-20, and are discussed in paragraph 9.2.

TABLE 6-15. ADVANCED MICRO DEVICES AM9140 ELECTRICAL CHARACTERIZATION - DC TESTS

PARAMETER	MIL-M-38510/237 TEST LIMITS		T_A = 25°C		T_A = 125°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.053	0.039	0.050	0.010	0.050	0.015	μAdc
I_{OHZ19}		10	1.366	2.150	2.645	2.672	2.125	2.287	μAdc
I_{OHZ20}		10	1.450	2.165	2.630	2.699	2.110	2.303	μAdc
I_{OHZ21}		10	0.894	0.768	2.065	1.739	1.625	1.900	μAdc
I_{OHZ26}		10	1.494	2.504	2.530	2.819	2.015	2.399	μAdc
I_{OLZ22}		10	0.055	0.016	0.090	0.015	0.070	0.025	μAdc
I_{OLZ23}		10	0.050	0.000	0.090	0.021	0.070	0.025	μAdc
I_{OLZ24}		10	0.055	0.016	0.090	0.021	0.070	0.025	μAdc
I_{OLZ25}		10	0.055	0.016	0.090	0.036	0.070	0.034	μAdc
I_{CC27}		125	50.222	7.953	37.750	7.096	50.050	16.266	mAdc
I_{CC28}		125	47.389	7.482	35.600	6.736	47.400	15.827	mAdc
I_{CC29}		89	35.000	6.210	26.750	5.213	34.950	11.677	mAdc
I_{CC30}		64	26.056	5.876	21.550	4.462	25.050	8.601	mAdc
V_{OH31}	2.2		3.978	0.136	3.908	0.128	3.952	0.158	Vdc
V_{OH32}	2.2		2.842	0.122	2.763	0.114	2.836	0.103	Vdc
V_{OL33}		0.4	0.137	0.015	0.192	0.025	0.146	0.056	Vdc
V_{OL34}		0.4	0.163	0.019	0.231	0.033	0.174	0.071	Vdc

TABLE 6-16. ADVANCED MICRO DEVICES AM9140 ELECTRICAL CHARACTERIZATION - FUNCTIONAL TESTS

PARAMETER	MIL-M-38510/237 TEST LIMITS		T_A = 25°C		T_A = 125°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_A		500							
GALPAT		↑	221.656	28.982	280.567	35.829	179.267	24.704	nS
GALWRT		↕	211.500	25.015	267.133	28.935	169.633	21.715	↕
WALKING		↕	223.312	29.084	284.037	36.783	179.800	24.752	↕
ROWPAT		↕	222.344	28.774	282.667	36.572	178.200	24.368	↕
MARCH		↕	222.875	28.821	283.567	36.718	178.833	24.420	↕
ADDCOMP		↕	221.875	28.934	285.200	28.135	178.267	24.564	↕
SHIFTING DIAGONAL		500 ↓	191.750	22.871	239.300	22.939	152.967	20.292	nS
t_W	200								
GALPAT	↑		41.813	8.442	53.300	8.059	32.200	7.670	nS
GALWRT	↕		42.000	8.821	53.467	8.172	32.300	7.651	↕
WALKING	↕		42.063	8.824	53.167	8.588	32.433	8.555	↕
ROWPAT	↕		41.969	8.557	53.600	8.164	32.233	7.800	↕
MARCH	↕		41.938	8.718	53.500	8.165	32.167	7.840	↕
ADDCOMP	↕		38.250	6.538	51.700	5.261	29.833	6.476	↕
SHIFTING DIAGONAL	200 ↓		41.781	8.298	54.867	5.904	31.967	7.190	nS

V_{CC} = 4.5 Vdc

TABLE 6-17. ADVANCED MICRO DEVICES AM9140 PATTERN EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PATTERN												
		T_A = 125°C							T_A = -55°C					
		GP	GW	W	R	M	A	SD	GP	GW	W	R	M	A	SD
READ/WRITE															
t_A	>900	100	100	100		100	50		100	100	100	50	100	50	
t_W	<300	100	100	100		100	50		100	100	100	50	100	50	
NUMBER OF DEVICE FAILURES AT T_A					2							2			

NOTES:

1. GP - GALPAT
   GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL

2. NO FAILURES AT T_A = 25°C

3. WORST CASE SUPPLY VOLTAGE: V_{CC} = 4.5V

TABLE 6-18. ADVANCED MICRO DEVICES AM9140 ELECTRICAL CHARACTERIZATION - DYNAMIC TIMING TESTS

PARAMETER	MIL-M-38510/237 TEST LIMITS		T_A = 25°C		T_A = 125°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_{CF}		200	81.467	0.890	95.472	5.806	82.564	6.869	nS
t_{CO}		220	98.933	13.254	137.752	26.184	83.171	17.248	nS
t_{DM}	0		16.667	10.575	13.616	20.081	16.471	11.874	nS
t_P		250	116.000	4.002	155.464	17.088	101.007	11.509	nS
t_{DS}	200		34.000	1.713	58.528	6.789	37.971	7.090	nS
t_{DH}	0		-20.333	0.597	-15.696	6.855	-18.864	2.309	nS
READ/MODIFY/WRITE									
t_A		500	221.400	9.623	270.408	34.121	174.250	26.192	nS
t_W	200		36.867	2.247	51.048	8.503	30.771	6.544	nS

V_{CC} = 4.75 Vdc

TABLE 6-19. ADVANCED MICRO DEVICES AM9140 DYNAMIC TIMING EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PARAMETER AND PATTERN T_A = 125°C				
		W	R	M	A	SD
READ/WRITE						
t_{CF}	>200	67	67	67	67	
t_{DM}	<320	33	33	33	33	
t_{DH}	<200	67	67	67	67	67
READ/MODIFY/WRITE						
t_A	>330	67	67	33	33	
PERCENT OF FAILED DEVICES DETECTED BY PATTERN		100	100	100	100	67
NUMBER OF FAILED DEVICES AT T_A				3		

NOTES:

1. W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL
2. NO FAILURES AT T_A = 25°C and T_A = -55°C
3. WORST CASE SUPPLY VOLTAGE: V_{CC} = 4.5V

TABLE 6-20. ADVANCED MICRO DEVICES AM9140 ELECTRICAL CHARACTERIZATION - THRESHOLD TESTS

PARAMETER	MIL-M-38510/235 TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{TH1}	-	-	1.587	0.074	1.527	0.067	1.674	0.076	Vdc
V_{THO}	-	-	1.472	0.080	1.381	0.071	1.510	0.104	Vdc

V_{CC} = 4.5 Vdc

6.4 MWS5501 TEST RESULTS

6.4.1 DC Parameters - Results of MWS5501 dc parameter tests are shown in Table 6-21. With the exception of the I_{DDH} and I_{DDL} parameters, the distribution of parameter values were well within the manufacturer's specified limits. The distribution of I_{DDH} and I_{DDL} values below one milliamp were also within the manufacturer's limits ($I_{DDH} \leq 500\,\mu A$ and $I_{DDL} \leq 200\,\mu A$), but approximately 30% of the parts displayed I_{DD} values greater than one milliamp at 85°C.

6.4.2 Functional Tests - Selected results of t_{RA} and t_W measurements performed while running functional tests with seven patterns are shown in Table 6-22. With the exception of the t_{RA} values obtained at 85°C while running the Walking pattern at 9.5 Vdc and 10.5 Vdc, there are no pattern-related variations in the 10 volt results. The values of t_{RA} obtained at 10 Vdc with the Walking pattern are slightly higher than the values obtained with the other six patterns for the reasons previously discussed.

The 5 Vdc results show a wide variation (20 nS) in the mean values of t_{RA} at 55°C. The maximum mean t_{RA} value of 152 nS was obtained with the Galpat pattern, and the minimum t_{RA} value of 132 nS was obtained with the Shifting Diagonal pattern.

A total of nine parts were also nonfunctional at 85°C with V_{DD} = 10.5 Vdc, and as shown in Table 6-23, were only detected with the Walking pattern. At -55°C, there were two nonfunctional devices with V_{DD} = 4.75 Vdc. Both of these failures were detected with a March pattern. One of the failures was also detected with the Addcomp pattern.

6.4.3 Timing Parameters - A summary of the timing parameter measurements is provided in Table 6-24. These measurements were performed at the lower voltage conditions (9.5 Vdc and 4.75 Vdc) where the access time parameter is

TABLE 6-21. RCA MWS5501 ELECTRICAL CHARACTERIZATION - DC TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		1.0	0.119	0.467	0.242	0.510	0.109	0.320	μAdc
I_{IL}		-1.0	0.004	0.259	-0.117	0.329	0.012	0.222	μAdc
I_{DDH}		500	53.460	41.844	151.933	55.800	43.454	52.913	μAdc
I_{DDL}		200	5.702	10.016	59.933	17.384	4.347	11.914	μAdc
V_{OH1}	-	-	9.497	0.029	9.495	0.035	9.497	0.030	Vdc
V_{OH2}	-	-	9.322	0.037	9.283	0.039	9.372	0.031	Vdc
V_{OH3}	-	-	4.617	0.018	4.584	0.021	4.662	0.012	Vdc
V_{OH4}	-	-	4.765	0.012	4.764	0.009	4.765	0.010	Vdc
V_{OL1}		0.1	0.005	0.016	0.006	0.017	0.005	0.016	Vdc
V_{OL2}		0.4	0.168	0.021	0.199	0.021	0.131	0.017	Vdc
V_{OL3}		0.4	0.159	0.044	0.180	0.017	0.120	0.015	Vdc
V_{OL4}		0.1	0.001	0.006	0.001	0.006	0.001	0.005	Vdc
$V_{IC(POS)}$	-	-	1.404	0.186	1.363	0.196	1.449	0.179	Vdc
$V_{IC(NEG)}$	-	-	-1.389	0.182	-1.350	0.193	-1.440	0.171	Vdc

TABLE 6-22. RCA MWS5501 ELECTRICAL CHARACTERIZATION - FUNCTIONAL TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_{RA}, 10.5V		125							
GALPAT		↑	75.304	6.382	83.923	5.851	68.190	6.284	nS
GALWRT		↕	73.130	5.294	81.615	5.122	63.333	4.714	↕
WALKING		↕	74.870	6.879	88.615	7.354	67.095	6.338	↕
ROWPAT		↕	75.348	6.491	83.769	5.925	67.571	6.344	↕
MARCH		↕	73.565	6.592	83.077	6.403	67.619	6.758	↕
ADDCOMP		↕	74.304	6.912	82.846	6.395	66.238	6.450	↕
SHIFTING		125	73.739	6.828	82.846	6.323	67.000	6.466	nS
DIAGONAL									
t_{RA}, 9.5V		125							
GALPAT		↑	81.130	6.956	89.769	6.303	73.048	6.168	nS
GALWRT		↕	76.652	5.631	85.538	5.473	66.000	5.004	↕
WALKING		↕	80.435	7.442	94.154	6.983	70.905	6.428	↕
ROWPAT		↕	80.652	6.806	89.154	6.274	72.571	6.366	↕
MARCH		↕	78.870	6.930	88.231	6.436	71.000	6.740	↕
ADDCOMP		↕	79.087	7.223	88.154	6.526	70.857	6.678	↕
SHIFTING		125	78.739	7.098	87.923	6.244	71.476	6.478	nS
DIAGONAL									
t_{RA}, 4.75V		250							
GALPAT		↑	154.478	16.030	167.769	14.733	152.333	19.308	nS
GALWRT		↕	154.130	16.200	168.692	15.158	135.048	12.117	↕
WALKING		↕	151.478	15.434	168.692	14.922	137.048	12.702	↕
ROWPAT		↕	154.435	15.767	167.846	14.507	144.238	16.177	↕
MARCH		↕	148.174	15.148	164.154	14.612	131.333	11.232	↕
ADDCOMP		↕	148.348	15.092	163.385	13.904	135.143	12.957	↕
SHIFTING		250	134.652	13.761	143.692	12.220	132.333	13.003	nS
DIAGONAL									
t_W, 10.5V	45								
GALPAT	↑		42.957	5.637	49.385	5.610	38.905	4.849	nS
GALWRT	↕		43.522	5.412	46.077	5.106	39.952	4.786	↕
WALKING	↕		44.609	6.232	50.692	6.330	38.952	4.806	↕
ROWPAT	↕		42.826	5.459	45.462	5.154	38.810	4.817	↕
MARCH	↕		42.130	5.335	45.231	4.870	39.095	4.946	↕
ADDCOMP	↕		41.870	5.472	45.385	5.241	38.667	4.754	↕
SHIFTING	45		42.957	5.520	45.615	5.001	39.429	4.797	nS
DIAGONAL									

TABLE 6-23. RCA MWS5501 PATTERN EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PATTERN													
		T_A = 85°C							T_A = -55°C						
		GP	GW	W	R	M	A	SD	GP	GW	W	R	M	A	SD
READ/WRITE															
t_{RA} V_{DD} = 10.5V	>260			100											
t_{RA} V_{DD} = 9.5V	>260			22											
t_{RA} V_{DD} = 4.75V	>260												100	50	
NUMBER OF DEVICE FAILURES AT T_A						9							2		
READ/WRITE															
t_W V_{DD} = 10.5V	<250			100											
t_W V_{DD} = 9.5V	<250			22											
NUMBER OF DEVICE FAILURES AT T_A						8									

NOTES:

1. GP - GALPAT
   GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL

2. NO FAILURES AT T_A = 25°C

TABLE 6-24. RCA MWS5501 ELECTRICAL CHARACTERIZATION - DYNAMIC TIMING TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{DD} = 9.5V									
READ/WRITE									
t_{DS}	30		9.792	0.971	10.593	1.140	8.510	0.936	nS
t_{DH}	30		17.292	4.068	18.850	3.839	17.531	3.876	nS
READ/MODIFY/WRITE									
t_{RA}		125	81.084	7.094	90.529	7.984	71.150	6.716	nS
t_W	45		45.968	6.241	50.243	6.737	41.204	5.312	nS
t_{DS}	30		9.942	0.982	10.729	1.133			nS
t_{DH}	30		17.305	4.062	18.921	3.843	17.531	3.874	nS
V_{DD} = 4.75V									
READ/WRITE									
t_{DS}	50		21.052	5.569	23.343	6.025	19.782	5.678	nS
t_{DH}	50		15.753	3.304	17.214	3.290	14.810	3.492	nS
READ/MODIFY/WRITE									
t_{RA}		250	150.877	16.592	162.950	17.712	139.395	17.398	nS
t_W	90		66.968	9.638	72.250	10.571	60.810	9.461	nS
t_{DS}	50		21.422	5.776	23.664	6.114	20.361	6.310	nS
t_{DH}	50		15.792	3.277	17.300	3.286	14.952	3.676	nS

typically the largest. However, in light of the pattern sensitivity problems noted at the high voltage condition, test specifications for these parts should include measurements at both the high and low voltage conditions using a Walking pattern. Examination of the mean and standard deviation of the timing parameter values shows that the distributions are within the manufacturer's specifications, although three failures were detected (two at 85°C and one at -55°C). As shown in Table 6-25, the 85°C failures were detected by only the Walking pattern, and the single -55°C failure was only detected by the March pattern. These results are in agreement with the functional test results.

6.4.4 Threshold Tests - Results of the threshold voltage tests are summarized in Table 6-26, and are discussed in paragraph 9.2.

TABLE 6-25. RCA MWS5501 DYNAMIC TIMING EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PARAMETER AND PATTERN												
		T_A = 85°C							T_A = -55°C					
		GP	GW	W	R	M	A	SD	GP	GW	W	R	M	A	SD
V_{DD} = 9.5V														
READ/WRITE														
t_{DS}	<200			100										
t_{DH}	<170			100										
READ/MODIFY/WRITE														
t_{RA}	>260			100										
t_W	<250			100										
t_{DS}	<170			100										
t_{DH}	<100			100										
V_{DD} = 4.75V														
READ/WRITE														
t_{DS}	<200													100
t_{DH}	<170													100
READ/MODIFY/WRITE														
t_{RA}	>260													100
t_W	<250													100
t_{DS}	<170													100
t_{DH}	<100													100
NUMBER OF FAILED DEVICES AT T_A				2							1			

NOTES:

1. GP - GALPAT
   GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL

2. NO FAILURES AT T_A = 25°C

TABLE 6-26. RCA MWS5501 ELECTRICAL CHARACTERIZATION - THRESHOLD TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{THP} V_{DD} = 9.5v	-	-	5.378	0.232	5.415	0.213	5.422	0.282	Vdc
V_{THN} V_{DD} = 9.5v	-	-	2.686	0.179	2.550	0.132	2.823	0.138	Vdc
V_{THP} V_{DD} = 4.75v	-	-	2.682	0.085	2.637	0.077	2.673	0.081	Vdc
V_{THN} V_{DD} = 4.75v	-	-	1.266	0.395	1.251	0.282	1.655	0.154	Vdc

6.5 CDP1821 TEST RESULTS

The CDP1821 is the microprocessor family designation for the MWS5501 memory, and is essentially the same chip. The CDP1821 is rated by the manufacturer as a 125°C part, but the 85°C limits for virtually all parameters have been relaxed to allow specification at 125°C. Comparison of the MWS5501 specification (85°C) with the CDP1821 specification (125°C) reveals that: a) I_{IH} has been increased from 1 μA to 10 μA, b) I_{DDH} has been increased from 500 μA to 1500 μA, and c) t_{RA} has been increased from 125 nS to 350 nS.

The dc parameter, functional, and timing parameter test results shown in Tables 6-27 through 6-31 are similar to those obtained with the MWS5501. Generally, the manufacturer's specification changes to permit 125°C operation appear warranted, but the magnitude of the changes may be excessive. MIL-M-38510 specification limits could probably be tighter than the manufacturer's catalog limits.

The extreme pattern sensitivity noted with the MWS5501 at high temperature and high voltage was not observed with the CDP1821. However, based on the two CDP1821 failures observed, it still appears that the Walking pattern is the most effective pattern for these parts.

TABLE 6-27. RCA CDP1821 ELECTRICAL CHARACTERIZATION - DC TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = 125°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.105	0.150	0.187	0.391	0.462	0.666	μAdc
I_{IL}		-10	0.041	0.054	-0.034	0.097	-0.297	0.145	μAdc
I_{DDH}		1500	78.124	54.602	204.200	120.681	523.600	195.693	μAdc
I_{DDL}		800	25.210	24.267	101.600	72.107	306.800	125.781	μAdc
V_{OH1}	-	-	9.520	0.000	9.514	0.010	9.510	0.010	Vdc
V_{OH2}	-	-	9.346	0.011	9.312	0.007	9.288	0.016	Vdc
V_{OH3}	-	-	4.630	0.011	4.598	0.012	4.582	0.009	Vdc
V_{OH4}	-	-	4.770	0.000	4.770	0.000	4.768	0.007	Vdc
V_{OL1}		0.1	0.018	0.004	0.018	0.004	0.020	0.000	Vdc
V_{OL2}		0.5	0.182	0.013	0.216	0.017	0.236	0.017	Vdc
V_{OL3}		0.4	0.157	0.020	0.185	0.022	0.205	0.025	Vdc
V_{OL4}		0.1	0.003	0.000	0.003	0.000	0.003	0.001	Vdc
$V_{IC(POS)}$	-	-	1.420	0.093	1.371	0.096	1.326	0.097	Vdc
$V_{IC(NEG)}$	-	-	-1.363	0.094	-1.319	0.098	-1.277	0.099	Vdc

TABLE 6-28. RCA CDP1821 ELECTRICAL CHARACTERIZATION - FUNCTIONAL TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = 125°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_{AA}, 10.5V		350							
GALPAT		↑	61.000	3.521	69.200	3.487	76.600	3.555	nS
GALWRT		↕	56.400	3.441	64.200	3.919	71.000	4.243	↕
WALKING		↕	59.800	3.125	70.400	2.653	83.400	4.842	↕
ROWPAT		↕	61.000	3.397	69.200	3.487	76.600	4.030	↕
MARCH		↕	59.000	3.347	66.600	2.938	77.200	5.193	↕
ADDCOMP		↕	60.000	3.950	68.200	3.599	76.000	3.950	↕
SHIFTING		350	59.800	3.869	68.200	3.486	76.600	3.136	nS
DIAGONAL									
t_{AA}, 9.5V		350							
GALPAT		↑	66.400	5.004	75.000	5.177	83.000	5.477	nS
GALWRT		↕	61.000	4.690	68.600	4.800	75.000	4.690	↕
WALKING		↕	65.000	4.604	76.600	4.758	90.800	5.308	↕
ROWPAT		↕	66.200	4.834	74.000	5.344	81.800	5.231	↕
MARCH		↕	63.000	4.100	72.200	4.215	85.400	6.312	↕
ADDCOMP		↕	62.800	4.579	71.000	3.950	79.000	3.949	↕
SHIFTING		350	65.400	5.004	73.000	4.858	81.400	4.799	nS
DIAGONAL									
t_{AA}, 4.75V		560							
GALPAT		↑	156.800	24.473	158.400	18.779	175.200	20.123	nS
GALWRT		↕	141.000	12.932	152.800	12.319	161.000	10.295	↕
WALKING		↕	146.600	18.250	169.600	16.836	209.600	21.464	↕
ROWPAT		↕	153.800	22.850	158.200	18.925	172.400	19.946	↕
MARCH		↕	137.600	14.208	150.800	14.810	168.000	18.176	↕
ADDCOMP		↕	142.000	15.925	152.400	14.178	177.800	15.767	↕
SHIFTING		560	139.000	17.574	147.000	13.070	173.400	15.653	nS
DIAGONAL									
t_W, 10.5V	140								
GALPAT	↑		36.000	0.633	38.800	1.166	43.800	1.166	nS
GALWRT	↕		36.200	0.748	39.000	1.265	41.800	1.166	↕
WALKING	↕		36.000	0.633	38.800	1.166	42.200	0.746	↕
ROWPAT	↕		35.800	0.748	38.600	1.019	44.400	1.200	↕
MARCH	↕		36.200	0.979	38.800	1.166	41.400	0.801	↕
ADDCOMP	↕		35.800	0.748	38.800	1.327	43.400	0.799	↕
SHIFTING	140		36.400	0.801	39.600	1.356	42.000	1.265	nS
DIAGONAL									

TABLE 6-29. RCA CDP1821 PATTERN EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PATTERN T_A = 25°C						
		GP	GW	W	R	M	A	SD
READ/WRITE								
t_{AA} V_{DD} = 5.25V	>260			100				
t_{AA} V_{DD} = 4.75V	>260	100		100				
NUMBER OF DEVICE FAILURES AT T_A					1			

NOTES:

1. GP - GALPAT
   GW - GALWRT
   W - WALKING
   R - ROWPAT
   M - MARCH
   A - ADDCOMP
   SD - SHIFTING DIAGONAL

2 NO FAILURES AT T_A = 85°C AND T_A = 125°C

TABLE 6-30. RCA CDP1821 ELECTRICAL CHARACTERIZATION - DYNAMIC TIMING TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 85°C		T_A = 125°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
V_{DD} = 10.5V									
READ/WRITE									
t_{AA}		350	63.050	3.486	71.500	3.542	79.700	5.041	nS
t_{DS}	140		10.550	0.589	11.500	0.592	12.650	0.963	nS
t_{DH}	56		9.750	0.433	9.900	0.300	10.100	0.436	nS
READ/MODIFY/WRITE									
t_{AA}		350	62.850	3.468	72.050	4.080	80.200	5.638	nS
t_{EN}		350	22.600	0.489	23.650	0.478	24.300	0.557	nS
t_W	140		35.600	0.917	40.000	1.549	44.800	1.832	nS
t_{DS}	140		8.950	0.740	9.900	0.625	11.150	0.853	nS
t_{DH}	56		9.750	1.043	10.050	0.805	10.650	1.062	nS
V_{DD} = 4.75V									
READ/WRITE									
t_{AA}		560	147.300	21.186	158.700	18.028	182.500	24.823	nS
t_{DS}	420		16.350	3.978	16.150	2.535	16.350	1.352	nS
t_{DH}	119		12.150	0.910	13.250	0.942	14.400	1.200	nS
READ/MODIFY/WRITE									
t_{AA}		560	146.400	20.365	157.750	17.490	182.650	24.874	nS
t_{EN}		560	32.900	1.641	34.900	1.546	36.350	1.389	nS
t_W	420		54.200	3.327	62.900	3.285	69.150	2.477	nS
t_{DS}	420		16.400	3.980	16.450	2.397	17.000	1.095	nS
t_{DH}	119		9.950	0.740	10.950	0.921	11.650	0.853	nS

TABLE 6-31. RCA CDP1821 DYNAMIC TIMING EFFECTIVENESS

PARAMETER	FAILURE CRITERIA nS	PERCENT FAILURE DETECTED BY PARAMETER AND PATTERN T_A = 25°C			
		GP	W	R	M
V_{DD} = 5.25V					
READ/MODIFY/WRITE					
t_{AA}	>250		100		
t_{DS}	< 50		100		
t_{DH}	< 50		100		
READ/MODIFY/WRITE					
V_{DD} = 4.75V					
t_{AA}	>250	100	100		
t_{DS}	< 50	100	100		
t_{DH}	< 50	100	100		
NUMBER OF FAILED DEVICES AT T_A			1		

NOTES:

1. GP - GALPAT
   W - WALKING
   R - ROWPAT
   M - MARCH

2. NO FAILURES AT T_A = 85°C and T_A = 125°C

6.6 CCD450 TEST RESULTS

The results of the limited testing (two devices) performed with the CCD450 dynamic shift register are summarized in Tables 6-32 through 6-34. In addition to the previously noted requirement for a 50 nS phase 2 clock rise time and possible sensitivity to the Altwor pattern, the CCD450 test results suggested that the parts do not meet the manufacturer's specification for t_{SW} and t_{SWD}. Since the CCD450 is no longer being manufactured, no further tests were performed.

TABLE 6-32. FAIRCHILD CCD450 ELECTRICAL CHARACTERIZATION - DC TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 55°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH1}		10	0.050	0.000	0.050	0.000	0.050	0.000	μA
I_{IH2}		2	1.300	0.000	1.150	0.000	1.180	0.035	mA
I_{IH3}		6	3.700	0.141	3.530	0.106	3.880	0.106	mA
I_{DD}		18	1.860	0.397	1.840	0.427	1.910	0.544	mA
I_{CC}		5000	0.493	0.033	0.445	0.026	0.463	0.015	μA
I_{BB}		10	-0.595	0.021	-0.470	0.000	-0.690	0.000	μA
V_{OH}	2.4		4.020	0.070	3.960	0.064	4.080	0.071	Vdc
V_{OL}		0.4	0.208	0.036	0.238	0.330	0.189	0.034	Vdc

AD-A079 627 MCDONNELL DOUGLAS ASTRONAUTICS CO ST LOUIS MO F/G 9/2
RELIABILITY EVALUATION AND ELECTRICAL CHARACTERIZATION OF MEMOR--ETC(U)
SEP 79 A T SASAKI F30602-77-C-0003
UNCLASSIFIED RADC-TR-79-193 NL

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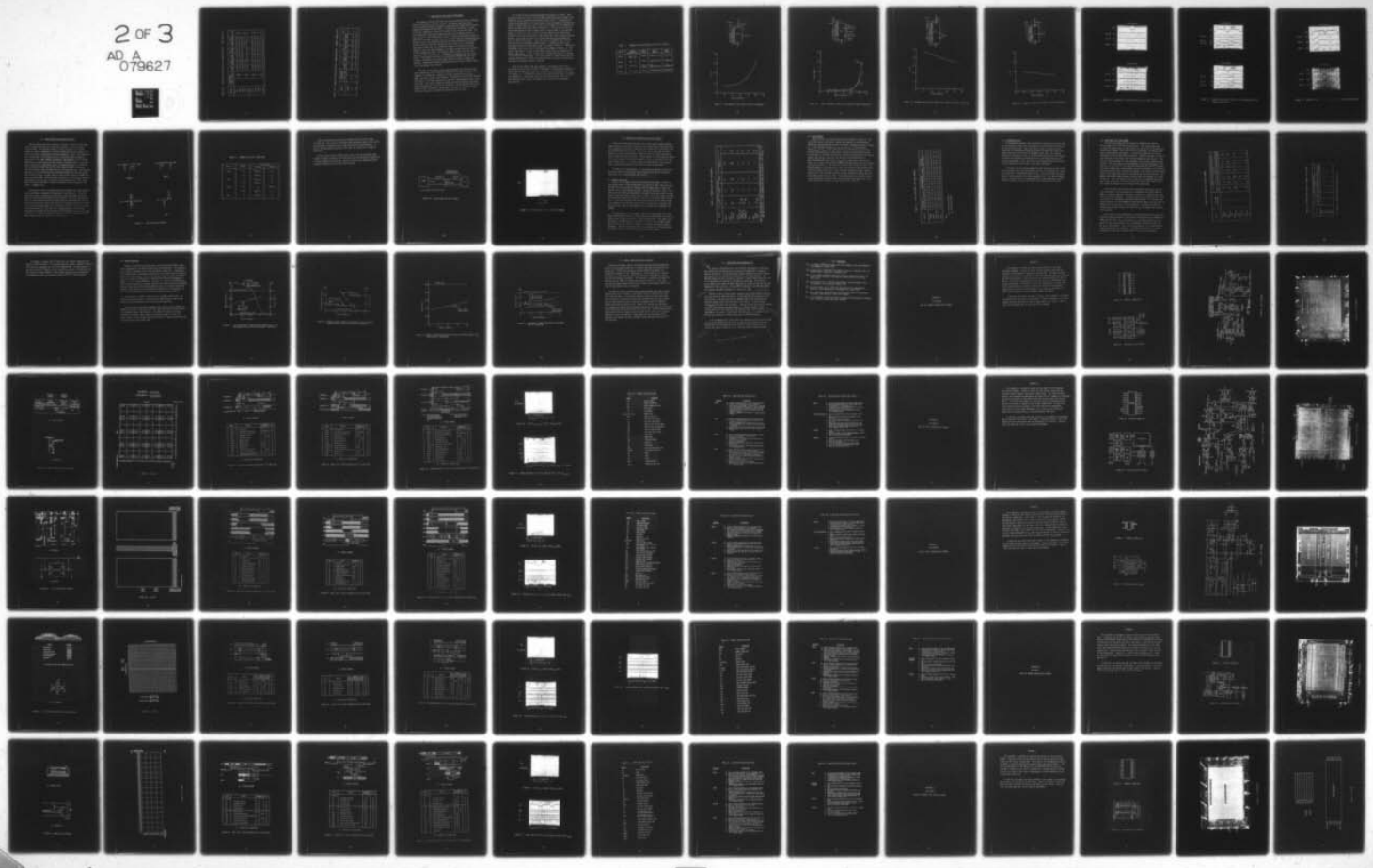


TABLE 6-33. FAIRCHILD CCD450 ELECTRICAL CHARACTERIZATION - FUNCTIONAL TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 55°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
$t_{RA(R/W)}$									
SCAN		180	135.500	5.657	151.500	4.243	129.250	3.889	nS
CBOARD1			136.750	5.303	152.500	4.243	130.500	2.828	
CBOARD2			137.000	4.950	164.250	20.577	130.200	3.818	
ALTWOR			137.000	4.950	-	-	130.200	3.818	
SRWALK		180	137.550	5.586	153.950	3.606	131.000	3.535	nS
$t_{RA(RMW)}$									
SCAN		180	135.500	5.657	151.000	4.950	129.000	3.536	nS
CBOARD1			136.550	5.586	152.000	4.950	130.550	2.899	
CBOARD2			136.800	5.233	152.050	4.879	130.250	3.182	
ALTWOR			137.000	4.950	152.500	4.243	130.850	3.323	
SRWALK		180	137.350	5.303	153.500	4.243	130.800	3.253	nS

TABLE 6-34. FAIRCHILD CCD450 ELECTRICAL CHARACTERIZATION - DYNAMIC TIMING TESTS

PARAMETER	MANUFACTURER'S TEST LIMITS		T_A = 25°C		T_A = 55°C		T_A = 0°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
t_{SW}	100		116.000	4.243	139.000	15.556	113.000	4.243	nS
t_{SWD}	50		64.000	1.414	105.500	62.933	69.000	2.828	nS

7.0 BURN-IN/LIFE TEST CIRCUIT EVALUATIONS

The purpose of the burn-in/life test circuit evaluations was to formulate effective MIL-M-38510 screening circuits. One dynamic and three static circuit configurations were evaluated by operating each memory type at ambient temperatures between 25°C and 125°C. Following this evaluation, a single circuit was selected for a burn-in/life test circuit verification test. The verification test consisted of operating three of each memory type for 72 hours at 125°C in the selected bias circuit. Electrical performance measurements after cool-down to room temperature with bias applied validated that the selected circuit was acceptable, and did not induce undesired failure modes. During the burn-in/life test evaluations, the criteria for an acceptable static bias circuit was: a) no thermal runaway, b) no excessive current densities, and c) no abrupt changes in an output voltage state over the 25°C to 125°C temperature range. An acceptable dynamic bias circuit was also required to meet these criteria. In addition, the memory must remain functional in the dynamic bias circuit at temperatures between 25°C and 125°C. During all evaluations, the device power supply and output voltages were recorded. Appropriate waveform photographs were also taken of memory operation in the dynamic bias circuits.

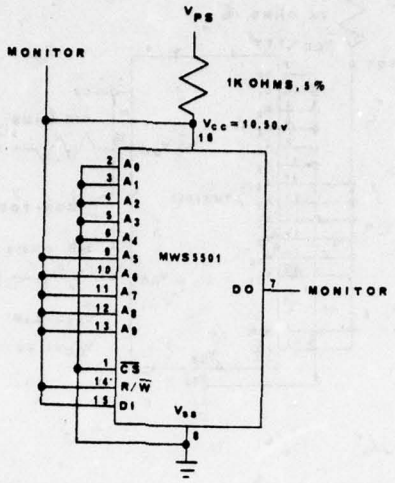
The three static burn-in circuits were selected from the device truth table combinations and included the read mode, write mode, and high output impedance or standby mode. Address pins were biased with V_{CC} and V_{SS} (GND), and device outputs were unloaded. The dynamic burn-in circuit operated the devices in the read/ modify/write mode with a checkerboard pattern, and a 30 pF load. This mode of operation closely approximates memory usage conditions and exercises all portions of the memory. During both the static and dynamic circuit evaluations, devices were stressed with the maximum rated operating voltage in the temperature range from 25°C to 125°C.

All of the circuits evaluated operated satisfactorily at 125°C. Thus, selection of burn-in circuits for MIL-M-38510 specifications was based on the electrical stress conditions established by each circuit. The dynamic bias circuits were selected for all memory types, since the electrical stresses are similar to usage conditions, and all parts of the memory will be subjected to maximum voltage stress pulses during the burn-in. Static bias circuits will not provide maximum voltage stresses across all gate oxides or pn junctions. However, a static bias test is felt to be more effective for accelerating failures due to ionic contamination, and perhaps both types of tests should be employed. Both types of tests are currently specified in MIL-M-38510 for Class "S" CMOS microcircuits. Thus, both static and dynamic test circuits were selected for the MWS5501 CMOS/SOS memory. A summary of the circuit conditions selected for each memory type is provided in Table 7-1. Details of the MWS5501 static bias circuit configuration are shown in Figure 7-1. Also shown in the figure is a plot of the supply current (I_{DD}) as a function of ambient temperature. Similar information is provided in Figures 7-2 through 7-4 for the other memory types. The circuits shown in these figures were the selected candidates for static bias configurations and could be useful where both static and dynamic biasing is desired.

Three of each memory type were operated in the dynamic bias circuit configuration for 72 hours at 125°C. Photographs of input/output waveforms of typical devices before and after the 72 hour burn-in are presented in Figures 7-5 through 7-7. Following the 72 hour circuit verification test, all devices were subjected to, and passed, electrical performance tests. Thus, all of the selected circuits appear satisfactory for inclusion in MIL-M-38510 specifications.

TABLE 7-1. SUMMARY OF SELECTED BURN-IN/LIFE TEST CIRCUITS

PART TYPE	MAXIMUM OPERATING VOLTAGE	TYPE OF CIRCUIT	MODE OF OPERATING	TEST PATTERN
TMS4050	VDD = 12.6V VBB = -5.5V	DYNAMIC	READ/MODIFY/WRITE	CHECKERBOARD
AM9140	VCC = 5.5V	DYNAMIC	READ/MODIFY/WRITE	CHECKERBOARD
MWS5501	VDD = 10.5V	STATIC DYNAMIC	READ READ/MODIFY/WRITE	N/A CHECKERBOARD
93481	VCC = 5.25V	DYNAMIC	READ/MODIFY/WRITE	CHECKERBOARD



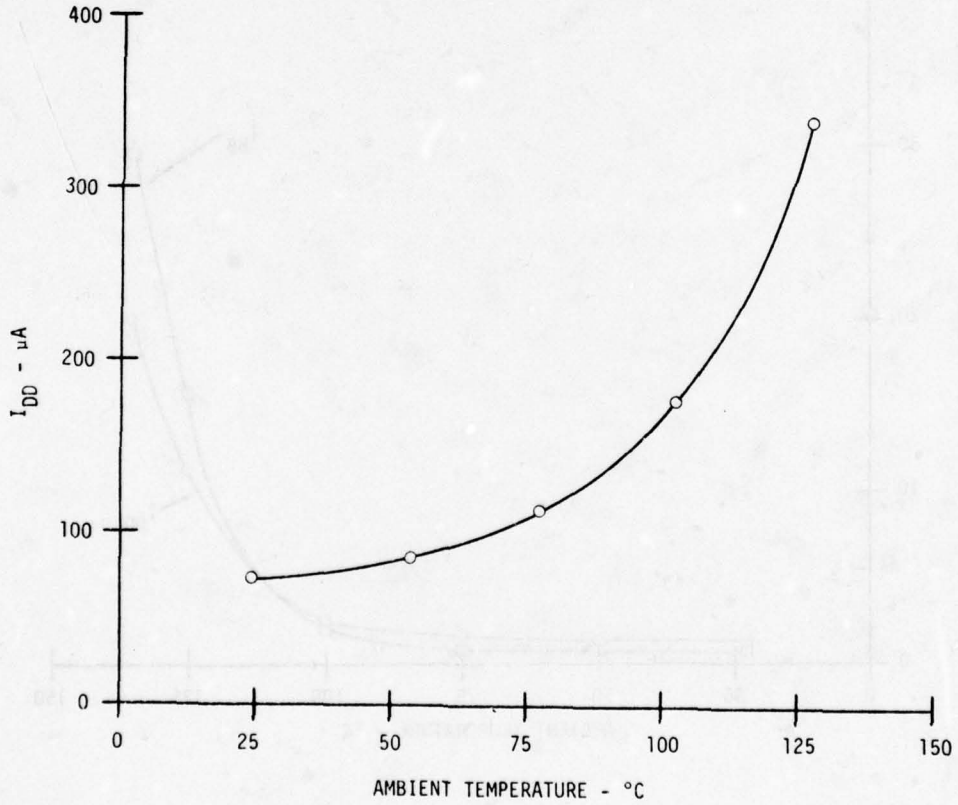
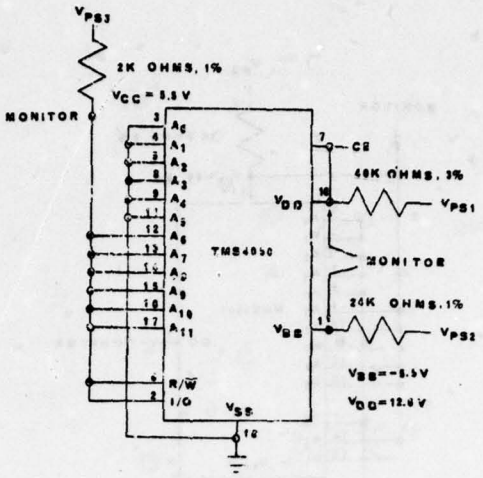


FIGURE 7-1. RCA MWS5501 STATIC BURN-IN CIRCUIT EVALUATION



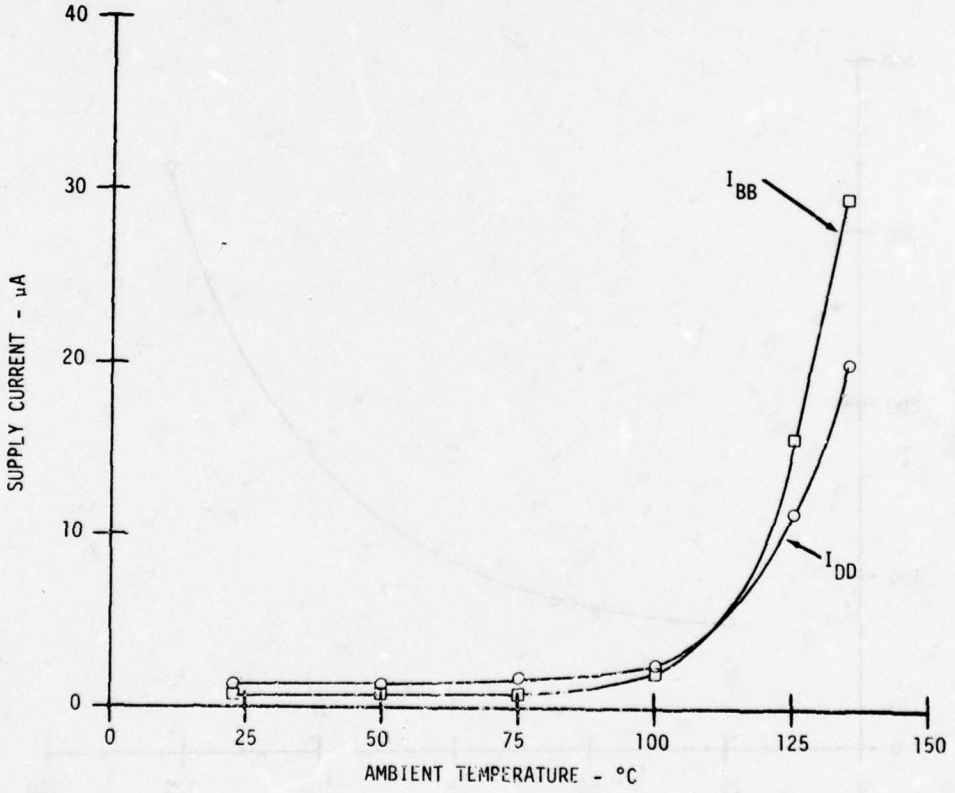


FIGURE 7-2. TEXAS INSTRUMENTS TMS4050 STATIC BURN-IN CIRCUIT EVALUATION

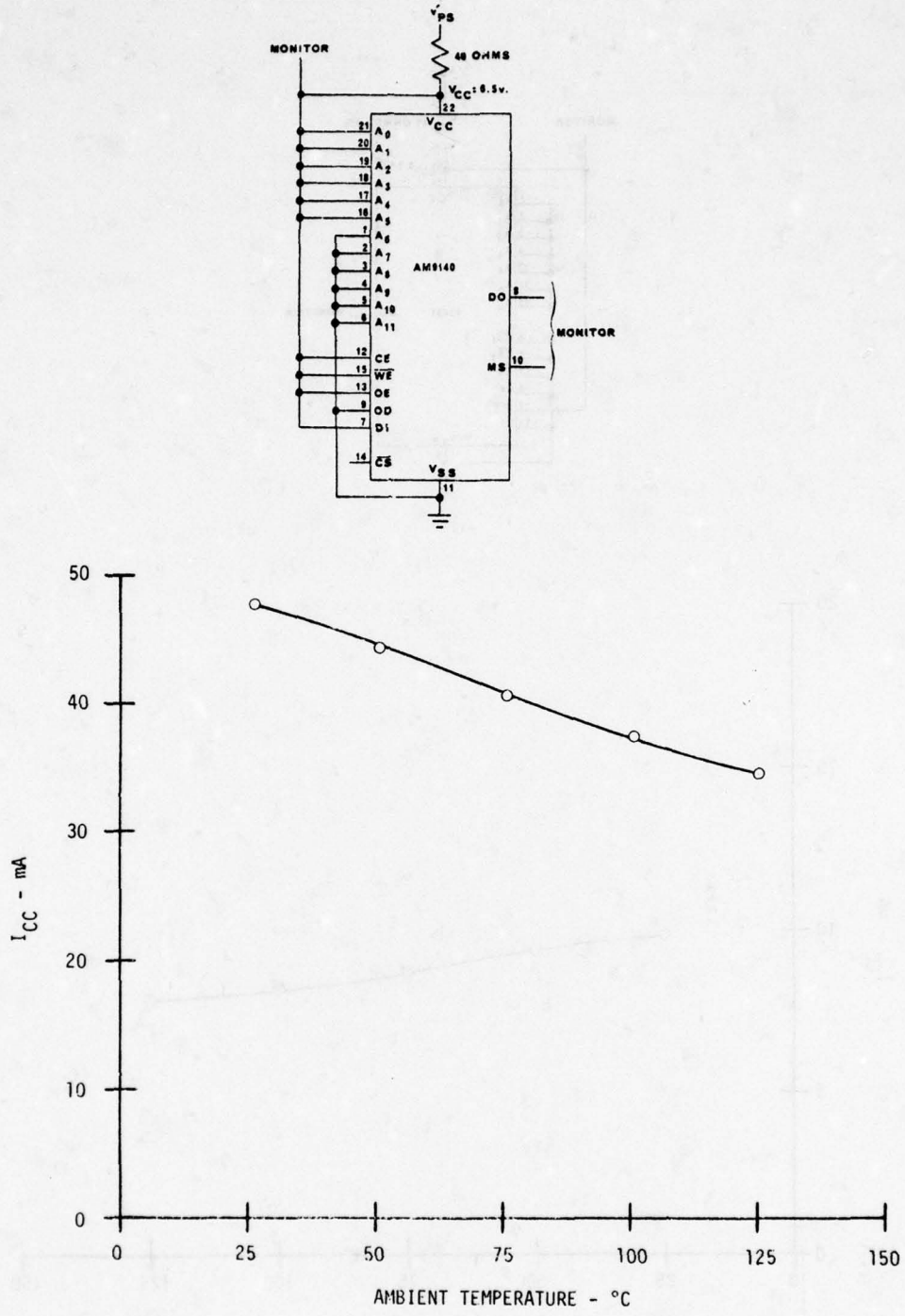


FIGURE 7-3. ADVANCED MICRO DEVICES AM9140 STATIC BURN-IN CIRCUIT EVALUATION

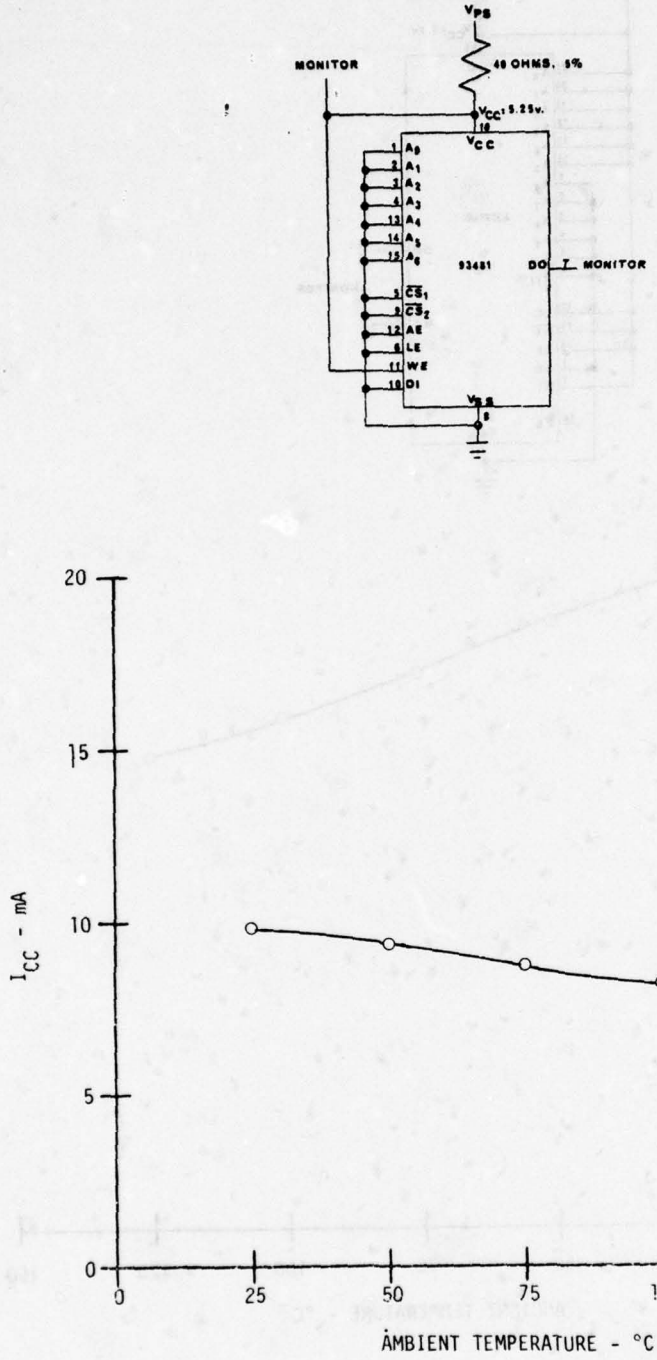


FIGURE 7-4. FAIRCHILD 93481 STATIC BURN-IN CIRCUIT EVALUATION

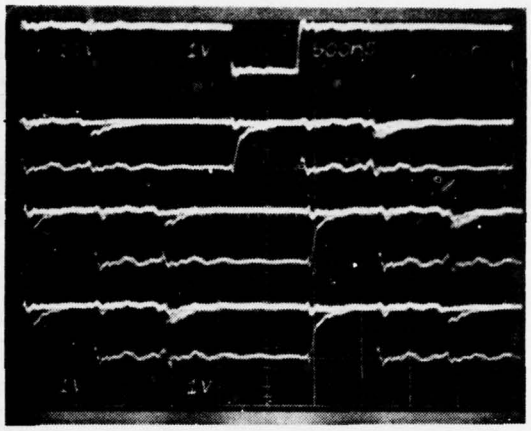
PRE BURN-IN

R/$\overline{W}$

S/N 53 DO

S/N 54 DO

S/N 63 DO



POST BURN-IN

R/$\overline{W}$

S/N 53 DO

S/N 54 DO

S/N 63 DO

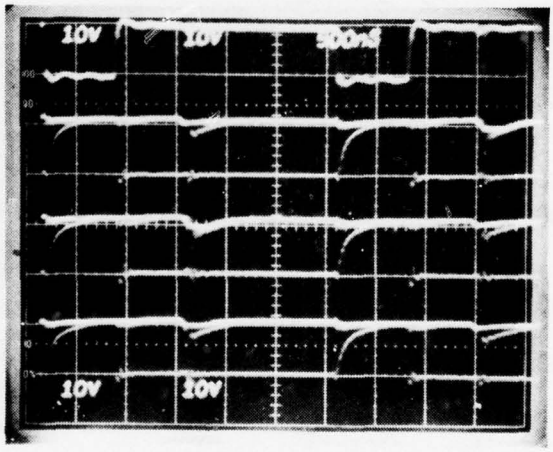
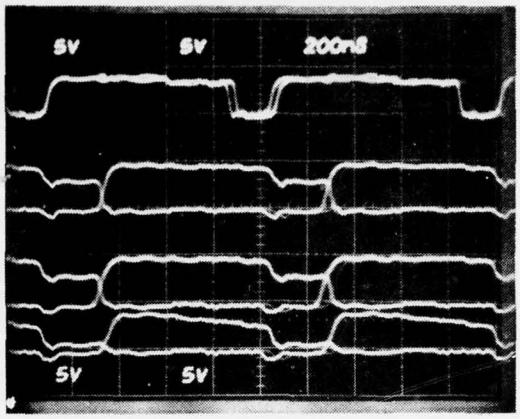


FIGURE 7-5. RCA MWS5501 72 HOUR BURN-IN/LIFE TEST CIRCUIT VERIFICATION

PRE BURN-IN



POST BURN-IN

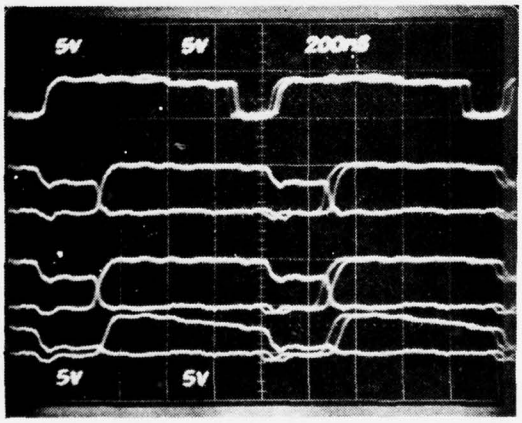
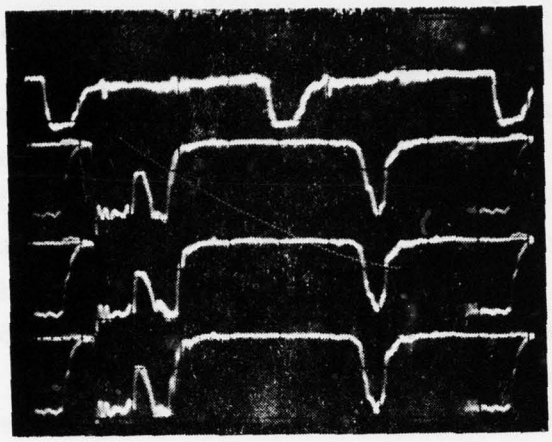


FIGURE 7-6. ADVANCED MICRO DEVICES AM9140 72 HOUR BURN-IN/LIFE TEST CIRCUIT VERIFICATION

PRE BURN-IN



POST BURN IN

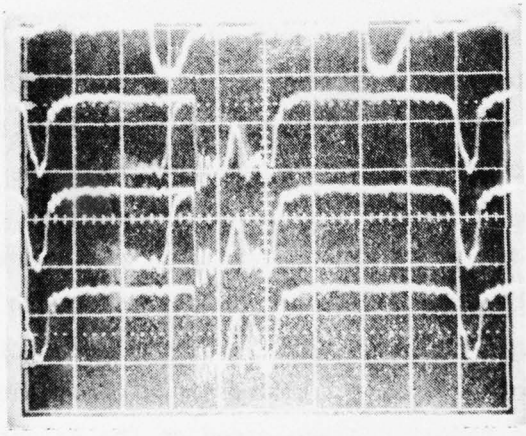
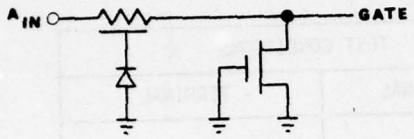


FIGURE 7-7. FAIRCHILD 93481 72 HOUR BURN IN/LIFE TEST CIRCUIT VERIFICATION

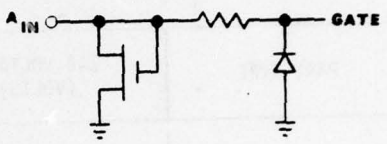
8.0 INPUT PROTECTION NETWORK EVALUATION

MOS and CMOS microcircuits normally incorporate circuitry at the input pins to protect the thin gate oxides from transient or static discharge induced damage. The networks typically include resistors, and clamping diodes or clamping transistors. Parasitic capacitors are also present, but may not be shown in manufacturer provided schematics. Input clamp diodes are also incorporated in TTL microcircuits for transient voltage protection. Examination of the NMOS (TMS4050 and AM9140), CMOS (MWS5501) and I^2L (93481) memory types revealed that the input protection networks shown in Figure 8-1 were incorporated in each memory type. No attempt was made to identify the input protection network for the CCD shift register (CCD450) since only limited evaluations were performed with this now obsolete part. Note that the CMOS input is protected from static discharges between the input and ground, and the input and V_{DD}. The NMOS memories only provide protection between the input pins and ground. Additional NMOS protection is not required, since the path between input and V_{DD} is normally a high impedance path. Thus, breakdown of the gate oxide due to transients between an input and V_{DD} will not result in damaged oxide.

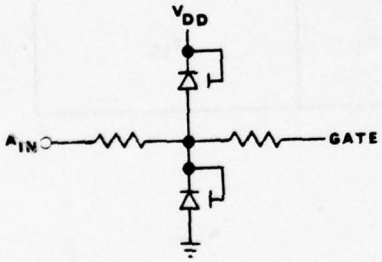
The degree of static discharge protection provided by the input networks can be evaluated by applying a voltage pulse to the input pin. The pulse should approximate in magnitude and duration a static discharge pulse that could be experienced during normal device handling. The worst case polarity that will cause damage to either the input stage or the protection circuitry should also be applied. Worst case polarity is the condition that will result in a reverse voltage breakdown of a pn junction since this results in maximum junction power/heating. The input pins, voltage polarities and voltage magnitudes established for testing memory input protection circuitry are shown in Table 8-1. Voltage magnitudes are based on the values contained in MIL-M-38510 specifications for the same or similar parts.



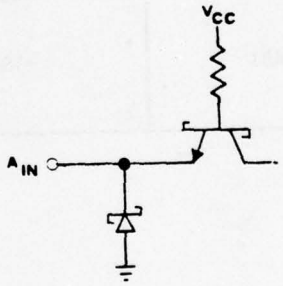
TMS4050



AM9140



MMS5501



93481

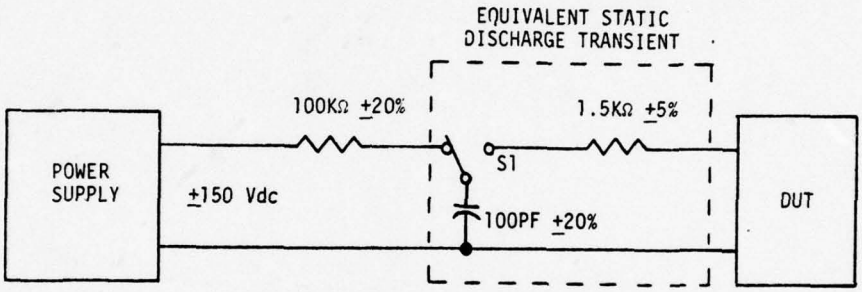
FIGURE 8-1. INPUT PROTECTION NETWORKS

TABLE 8-1. SUMMARY OF ZAP TEST CONDITIONS

PART TYPE	ZAP VOLTAGE (VOLTS)	TEST CONDITIONS	
		+ TERMINAL	- TERMINAL
TMS4050	+150	ADDRESS A_0	V_{SS}
	-150	ADDRESS A_0	V_{SS}
AM9140	+150	ADDRESS A_0	V_{SS}
	-150	ADDRESS A_0	V_{SS}
MWS5501	+400	V_{DD}	ADDRESS A_0
	+400	ADDRESS A_0	V_{SS}
93481	+150	ADDRESS A_0	V_{SS}

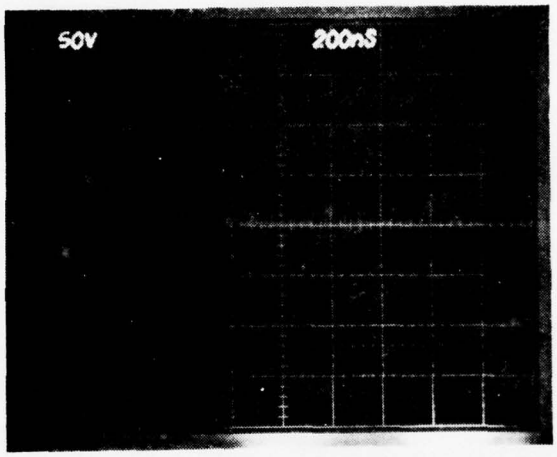
Static discharge-type pulses were simulated with the circuit shown in Figure 8-2. The values of resistances and capacitance shown in the circuit were selected to represent typical body resistance and capacitance [6]. A typical voltage waveform obtained at the input of a device pin is shown in Figure 8-3.

Following the static discharge (Zap) tests of two of each memory type (CCD450 excluded), parametric and functional tests were performed to determine if device damage was experienced. Results of these tests showed negligible parameter degradation and no functional failures.



S1 = Hg wetted "chatter free" relay.

FIGURE 8-2. HIGH VOLTAGE ZAP TEST CIRCUIT



V_{ZAP}

t

$\tau = .15\ \mu s$

$V_{(5\tau)} \approx 0V$

FIGURE 8-3. HIGH VOLTAGE ZAP TEST DISCHARGE VOLTAGE

9.0 ANALYSIS OF CHARACTERIZATION TEST RESULTS

Electrical characterization test results were used to compute maximum power dissipation and noise immunity for each memory type. The results were also analyzed in an attempt to determine the optimum set of electrical tests for a MIL-M-38510 specification. The optimum set of tests was initially defined to be the minimum number of tests (minimum test time) required to obtain a 90% test confidence level. Unfortunately, for large memories (RAMs), it is not practical to verify the integrity of all, or even 90% of all possible signal paths, as is typically done with combinatorial logic devices. Thus, a qualitative analysis of test effectiveness was performed.

Included in this section are: a) the results of the power dissipation and noise immunity calculations, and b) discussions of the dc parameter, functional, and timing parameter test results.

9.1 POWER DISSIPATION

Results of the power dissipation calculations are shown in Table 9-1. The average values of the maximum power dissipation at each temperature were obtained from the products of average values of power supply current and maximum value of power supply voltages. The worst case values shown in the table were calculated as the product of average plus 3 sigma values of power supply current and maximum power supply voltage. Worst case values are shown for the ambient temperature condition that results in maximum power dissipation. All of the calculated power dissipation values are for the quiescent state, however, for reference, typical 25°C catalog values of dynamic power dissipation are shown for the CMOS/SOS and CCD memory types (MWS5501, and CCD450).

The CMOS/SOS memory, as expected, requires the least power of all the memory technologies evaluated. Ranking the other technologies from lowest to highest power dissipation results in the following order: CCD, NMOS static, I^2L dynamic, and NMOS dynamic. In light of the fact that the NMOS dynamic RAM is a 12 Vdc part and the I^2L RAM is a 5 Vdc part, the ranking appears reasonable. The worst case power dissipation values are also approximately the manufacturer's, or MIL-M-38510, specified maximum values.

TABLE 9-1. MEMORY DEVICE POWER DISSIPATION

PART TYPE	MAXIMUM POWER DISSIPATION-AVERAGE			MAXIMUM POWER DISSIPATION WORST CASE	UNITS
	T_A = 25°C	HI TEMP	LO TEMP		
TMS4050	631	475	827	1024	mW
AM9140					
CHIP ENABLE	276	207	275	544	mW
PWR DOWN	143	119	138	280	mW
MNS5501					
QUIESCENT (10V)	0.6	1.6	0.5	2.1	mW
DYNAMIC (10V)	60 ①	-	-	-	
QUIESCENT (5V)	0.06	0.6	0.05	0.4	mW
DYNAMIC (5V)	18 ①	-	-	-	
93481	431	421	431	552	mW
CCD450					
QUIESCENT	23	23	24	-	mW
DYNAMIC	176 ②	-	-	-	mW

NOTES: ① POWER DISSIPATION IS ESTIMATED FROM MANUFACTURER CATALOG SPECIFICATIONS WITH C_L = 30 pF AND t_{cyc} = 400 nS.
② POWER DISSIPATION IS ESTIMATED FROM MANUFACTURER CATALOG SPECIFICATIONS WITH C_L = 50 pF AND t_{cyc} = 1 µS.

9.2 NOISE MARGINS

Results of the noise margin calculations are shown in Table 9-2. The static RAM typical noise margin figures were computed as the difference between the average measured values of threshold voltages and output voltages. V_{NL} is the difference between V_{THO} and V_{OL}, and V_{NH} is the difference between V_{OH} and V_{TH1}. Worst case values of static RAM noise margins were computed using the mean ± 3 sigma values yielding the minimum noise margin. The same general technique was used for calculating dynamic RAM noise margins. However, V_{OH} and V_{OL} values were not measured and the manufacturer's specified maximum/minimum values of V_{OH} and V_{OL} were used in the calculations. As a result, the calculated TMS4050 and 93481 worst case noise margins are highly pessimistic. The low value of noise margin (0.06 volts) for the CMOS/SOS memory is also pessimistic, and is attributed to the apparent large variation (sigma $\approx$ 0.44 volt) in the n-channel threshold voltage. However, examination of the n-channel threshold voltage distribution showed that most values were greater than one volt. Since noise margins are verified implicitly by performing functional tests with maximum/minimum input level logic states, additional threshold voltage tests are not required.

TABLE 9-2. TYPICAL AND WORST CASE NOISE MARGINS

PART TYPE	MANUFACTURER'S TEST LIMITS		TYPICAL NOISE MARGIN						WORST CASE NOISE MARGIN		UNITS
			T_A = 25°C		HI TEMP		LO TEMP				
	V_{NL}	V_{NH}	V_{NL}	V_{NH}	V_{NL}	V_{NH}	V_{NL}	V_{NH}	V_{NL}	V_{NH}	
TMS4050	0.200	0.200	0.575	0.647	0.530	0.758	0.590	0.714	0.000	0.128	Vdc
AM9140	0.400	0.200	1.309	1.255	1.150	1.236	1.336	1.162	0.811	0.625	Vdc
MWS5501 (10V)	2.000	2.000	2.681	4.119	2.544	4.080	2.818	5.422	2.096	3.139	Vdc
MWS5501 (5V)	1.000	1.000	1.265	2.083	1.250	2.127	1.654	2.092	0.062	1.792	Vdc
93481	0.300	0.300	0.646	0.521	0.518	0.729	0.799	0.300	0.307	0.000	Vdc

NOTES:

1. V_{NL} = LOW LEVEL NOISE MARGIN

   V_{NH} = HIGH LEVEL NOISE MARGIN

9.3 DC PARAMETER TESTS

The selected dc parameter tests represent the minimum set of tests that can be performed to ensure that dc parameters are within specified limits at all operating conditions. Additional tests at other voltage and current conditions are unnecessary because the selected voltage/current conditions produce the worst case value of the parameter under test. The selected sequence of performing dc tests is also believed to be optimum since temperature sensitive parameters are measured prior to performing high power dissipating measurements. Thus, test time is not wasted waiting for the device to reach thermal equilibrium after a high power measurement.

In general, the test results showed that the distribution of most parameter values were within the manufacturer's limits, and tightened limits could be incorporated in MIL-M-38510 specifications. Only one instance was noted where all parts exceeded a particular parameter limit. This was the TMS4050 I_{DD}(CEL) parameter, and it is recommended that the MIL-M-38510/235 specification be revised to reflect the results of this characterization study.

9.4 FUNCTIONAL TEST EFFECTIVENESS

The functional test data was analyzed to determine the relative effectiveness of N^2, $N^{3/2}$ and N type patterns. Two criteria were used to judge the effectiveness of each pattern: a) the ability of the pattern to detect memory defects, and b) the ability of the pattern to produce a worst case timing parameter measurement. A pattern that meets both criteria is considered to be the most effective pattern. Table 9-3 provides a summary of the percentage of functional test failures detected by each pattern. Also shown are the percentage of timing parameter test failures detected by each pattern. With one exception, the percentage of failures detected by N type patterns was equivalent to the percentage detected by N^2, and $N^{3/2}$ patterns. This would suggest that N type patterns are just as effective as N^2 patterns. Unfortunately the nature of the device defects is not known, and there may be other failure modes that would not be detected by the N type patterns. The MWS5501 and CDP1821 CMOS/SOS memory failures were only detected by a single N^2 pattern. Thus, the results of this study are not considered conclusive. High volume electrical test results containing both N^2 and N type pattern data should be examined prior to forming final conclusions.

Table 9-4 shows the pattern(s) that produced the worst case values of timing parameters. With the exception of the MWS5501 and CDP1821 CMOS/SOS RAMs, all patterns appeared to be equally effective in producing worst case values of timing parameters. The Walking pattern was clearly the most effective pattern for the MWS5501 and CDP1821 CMOS/SOS RAMs. All patterns were equally effective for the TMS4050 and 93481 dynamic RAMs, with less than 2 nS pattern-related variation in timing parameters. The Galwrt and Shifting Diagonal pattern were slightly less effective for the AM9140 than the other five patterns.

Discussions with the manufacturers concerning patterns used during their electrical testing revealed: a) both dynamic RAM manufacturers (TMS4050 and 93481) use N^2, $N^{3/2}$, and N type patterns, b) the AM9140 manufacturer uses only $N^{3/2}$ and N type patterns, and c) the MWS5501 manufacturer uses only N^2, and N type patterns. Thus, only one manufacturer is not performing N^2 type pattern tests on a 100% basis. The 93481 manufacturer is currently reviewing his data, and it appears that N^2 tests are not necessary.

TABLE 9-3. PATTERN EFFECTIVENESS SUMMARY

PART TYPE	TOTAL NUMBER OF FAILED DEVICES	PERCENT OF FAILED DEVICES DECTCTED BY PATTERN						
		N^2			$N^{3/2}$	N		
		GALPAT	GALWRT	WALKING	ROWPAT	MARCH	ADDCOMP	SHIFTING DIAGONAL
TMS4050								
FUNCTIONAL	8	88	75	88	75	88	75	100
TIMING	11	N/A	82	91	91	91	82	N/A
93481								
FUNCTIONAL	6	100	100	100	100	100	100	100
TIMING	9	100	N/A	N/A	89	89	78	67
AM9140								
FUNCTIONAL	4	100	100	100	25	100	75	0
TIMING	3	N/A	N/A	100	100	100	100	100
MWS5501								
FUNCTIONAL	9	0	0	100	0	0	0	0
TIMING	3	0	0	67	0	33	0	0
CDP1821								
FUNCTIONAL	1	100	0	100	0	0	0	0
TIMING	1	100	N/A	100	0	0	N/A	N/A

TABLE 9-4. PATTERNS THAT RESULTED IN WORST CASE TIMING

PART TYPE	WORST CASE TIMING MEASURMENT						
	N^2			$N^{3/2}$	N		
	GALPAT	GALWRT	WALKING	ROWPAT	MARCH	ADDCOMP	SHIFTING DIAGONAL
TMS4050	X	X	X	X	X	X	X
93481	X	X	X	X	X	X	X
AM9140	X		X	X	X	X	
MWS5501			X				
CDP1821			X				

NOTE: MULTIPLE "X"s INDICATE THE PATTERNS ARE EQUALLY EFFECTIVE.

In summary, it appears that N^2 type tests are probably unnecessary for the 4K bit RAMs included in this characterization program. However, a Walking (N^2) pattern is necessary for the 1K bit CMOS/SOS RAM. The manufacturer of this part uses an N^2 pattern, but not the Walking pattern. The necessity for N^2 patterns to detect defects in other memory types can only be determined from comparative tests using several types of N^2, $N^{3/2}$, and N patterns.

9.5 TIMING PARAMETERS

Analysis of the timing parameter data, as previously mentioned, showed little dependence on the pattern used during the measurements. The parameters were, however, dependent upon voltage and ambient temperature. Consequently, all timing parameter measurements were made at the voltage condition producing worst case timing values. Plots of the average values of access and refresh time as a function of temperature illustrated the temperature dependence of these critical timing parameters. Figure 9-1 is a plot of the TMS4050 parameters versus temperature, and shows that both are highly temperature dependent. The worst case condition for both parameters occurs at the upper temperature extemes, since refresh time is decreasing and access time is increasing. At 85°C, the average refresh time is 23 mS and the access time is 173 nS.

A similar plot is shown in Figure 9-2 for the 93481 dynamic RAM. The refresh time characteristic is similar to the TMS4050 dynamic RAM, but the access time curve indicates little variation with temperature.

Plots of access time versus temperature for the static RAMs (AM9140 and MWS5501) are shown in Figures 9-3 and 9-4. Both memory types exhibit temperature dependent access time parameter. The effects of operating voltage variations on MWS5501 access time is also clearly evident in Figure 9-4. Access time at the low voltage condition (4.75 Vdc) is approximately twice the high voltage (9.5 Vdc) access time.

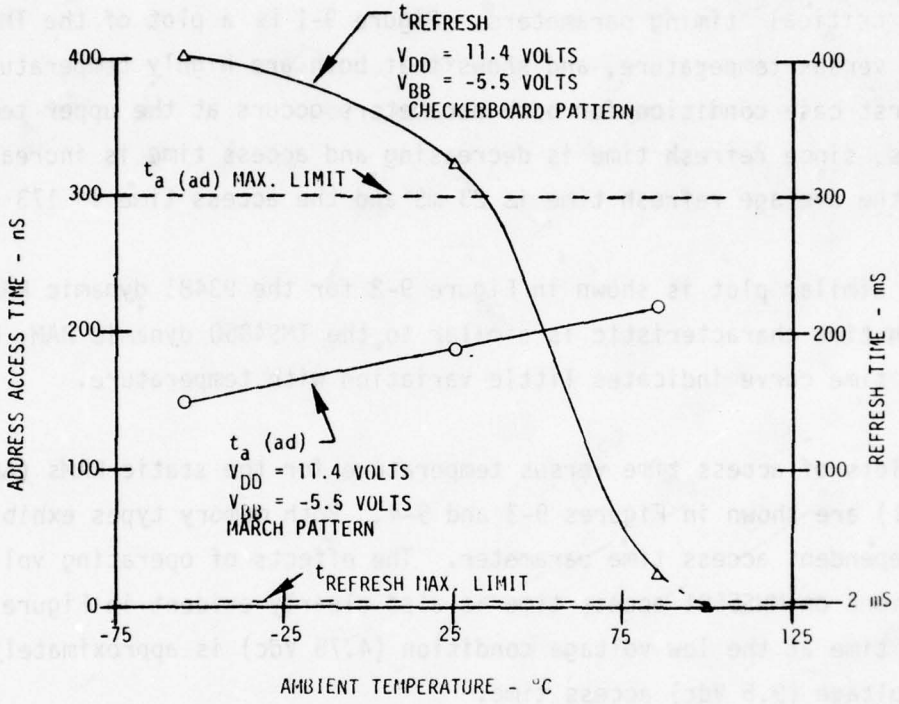


FIGURE 9-1. TEXAS INSTRUMENTS TMS4050 AVERAGE ADDRESS ACCESS TIME AND AVERAGE REFRESH TIME VERSUS AMBIENT TEMPERATURE

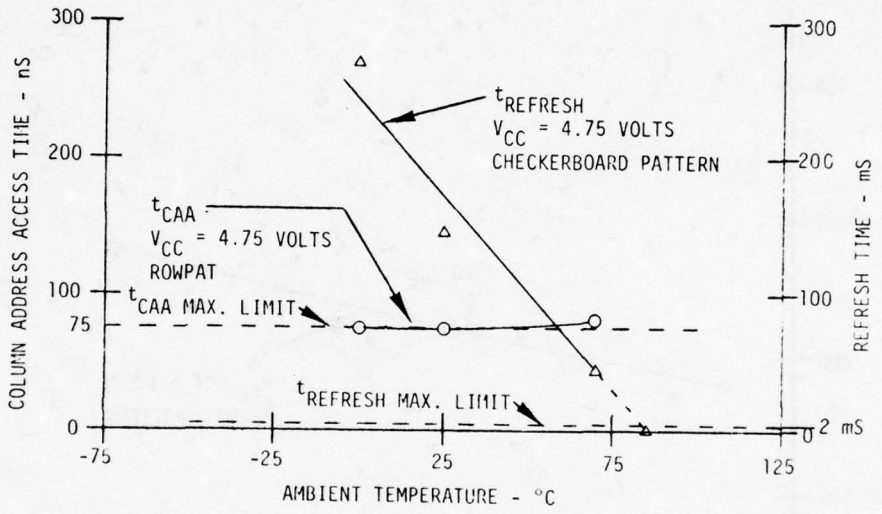


FIGURE 9-2. FAIRCHILD 93481 AVERAGE COLUMN ADDRESS ACCESS TIME AND AVERAGE REFRESH TIME VERSUS AMBIENT TEMPERATURE

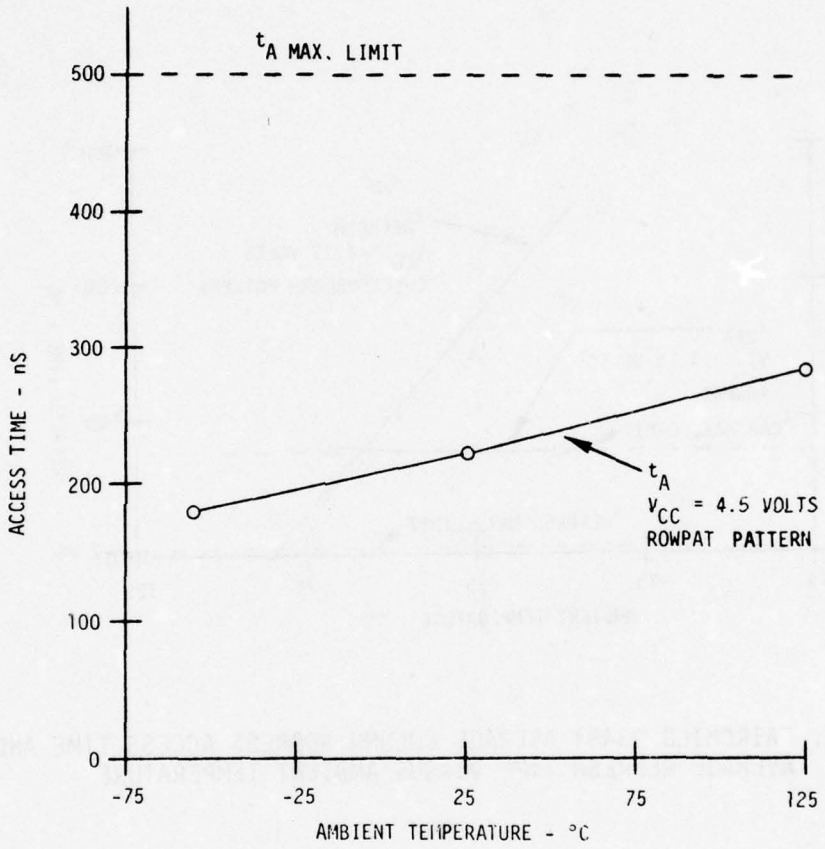


FIGURE 9-3. ADVANCED MICRO DEVICES AM9140 AVERAGE CHIP ENABLE ACCESS TIME VERSUS AMBIENT TEMPERATURE

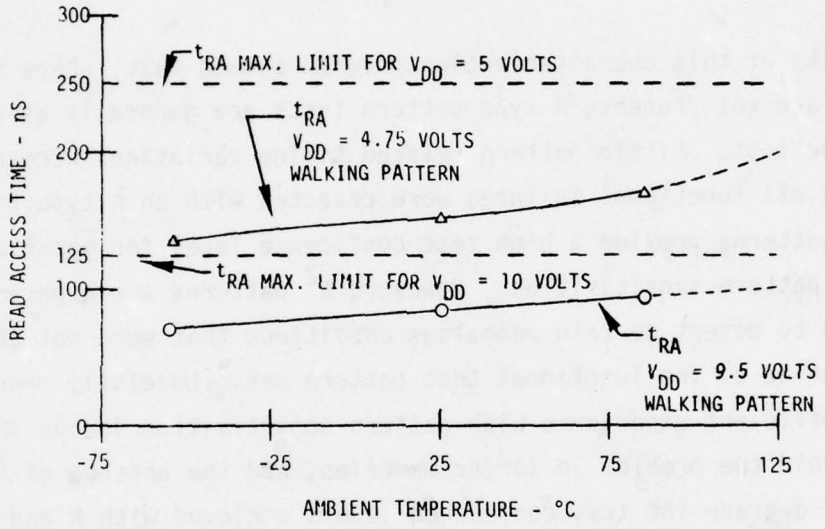


FIGURE 9-4. RCA MWS5501 AVERAGE READ ACCESS TIME VERSUS AMBIENT TEMPERATURE

10.0 MEMORY CHARACTERIZATION PHILOSOPHY

The basic philosophy used for this memory characterization program was similar to the procedure developed in previous RADC memory characterization studies [7]. Briefly this procedure involved checking the memory for: a) address uniqueness, b) bit independence, c) cell integrity, d) intercell disturbance, e) data retention and f) the ability of the memory to recover from various read/write sequences. This procedure is generally accepted and has been used for RAMs with memory capacities up to 4K bits. Test times using this procedure become prohibitive for memory sizes greater than 4K bits, since N^2 type pattern tests are required.

The results of this characterization program showed that, where pattern sensitivities are not present, N type pattern tests are generally as effective as N^2 type test. Little pattern related timing variations were noted, and, virtually all functional failures were detected with an N type pattern. Thus, N type patterns provide a high test confidence level for memories without major pattern sensitivities. However, N^2 patterns are apparently still required to detect certain anomalous conditions that were not anticipated during formulation of the functional test pattern set. Hopefully manufacturers have gained sufficient experience with pattern sensitivities in the smaller memories to avoid the problem in larger memories, and the absence of N^2 tests will not degrade the test confidence levels achieved with N and $N^{3/2}$ test patterns.

11.0 CONCLUSIONS AND RECOMMENDATIONS

LSI memories implemented with five different semiconductor technologies were electrically characterized as a function of temperature, voltage and pattern sensitivity. No new technology related characteristics were revealed that would limit the performance characteristics of these memories. The CMOS/SOS memory was the only device to exhibit a pattern sensitivity, but this is not believed to be related to the CMOS/SOS technology. Only the two static memory types (NMOS and CMOS) exhibited the capability for full military temperature range operation, and the 85°C performance of the CMOS/SOS memory was severely degraded (although still useful) at 125°C.

Studies of pattern effectiveness suggested that N type patterns could be used for electrical characterization. Except where N^2 pattern sensitivities are present, as was the case with the CMOS/SOS RAM, little difference was observed between the N^2 and N functional test results. Pattern related timing variations were also negligible. Although efforts were made to identify N or $N^{3/2}$ type patterns that would detect all types of defects, an N^2 pattern sensitivity was detected in the CMOS/SOS RAM. Without specific knowledge of the nature of the CMOS/SOS RAM deficiency, it is apparent that N^2 tests are necessary to detect these types of RAM deficiencies.

It is recommended that future electrical characterization studies include provisions for determining the nature of observed device deficiencies. Discussions with the manufacturer are helpful in some instances, but are usually not specific enough to aid in resolving pattern related problems.

12.0 REFERENCES

[1] J. Cocking, "RAM Test Patterns and Test Strategy," 1975 Semiconductor Test Symposium, October 1975.

[2] C. Kuo, et al, "Sense Amplifier Design Is Key to 1-Transistor Cell in 4096-Bit RAM," Electronics, September 1973.

[3] J. H. Kroeger, "Designing with Self Clocking, Adaptive 4K Static R/W Random Access Memories," Advanced Micro Devices Application Note, April 1976.

[4] G. Panigrahi, et al, "Charge Coupled Memory Test Philosophy," 1975 Semiconductor Test Symposium, October 1975.

[5] S. Firoz Husain, et al, "Military Specification for Semiconductor Memories," 1975 Semiconductor Test Symposium, October 1975.

[6] R. J. Antinone, "Specifications for Microciuit Electrical Overstress Tolerance," RADC-TR-78-28, March 1978, A052814.

[7] T. M. Ostrowski, "Characterization of Complex Microprocessor and Support Chips," RADC-TR-78-138, June 1978, A057079.

APPENDIX A

P/N TMS4050

4096 BIT DYNAMIC RANDOM ACCESS MEMORY

APPENDIX A

This appendix is included to supply various details of the Texas Instruments TMS4050. Figures A1 and A2 are the terminal layout and the functional block diagram of the device, respectively. The Figure A3 logic diagram, the Figure A4 die photograph, the Figure A5 transistor cell structure and the bit map shown in Figure A6 provide even greater layout and function detail. The timing requirements for the read, write, and read/modify/write cycles are provided in Figures A7, A8, and A9, respectively. Further electrical characteristics are shown in the Figure A10 and A11 photographs. Figure A10 is a curve tracer photograph of I_{DD} versus V_{DD} and Figure A11 shows several waveforms during an address access time cycle.

In addition, two tables have been included in this appendix to supplement the discussion of this device in the report. Table A1 provides a list of the symbols and their definitions that are applicable to this device. Table A2 lists the algorithms used in this study of the TMS4050.

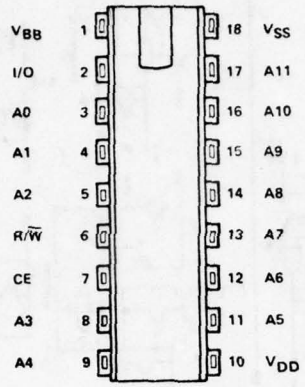


FIGURE A1. TERMINAL CONNECTION

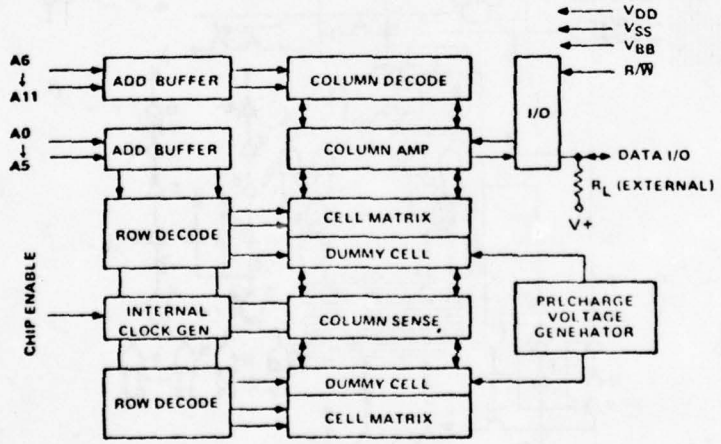


FIGURE A2. FUNCTIONAL BLOCK DIAGRAM

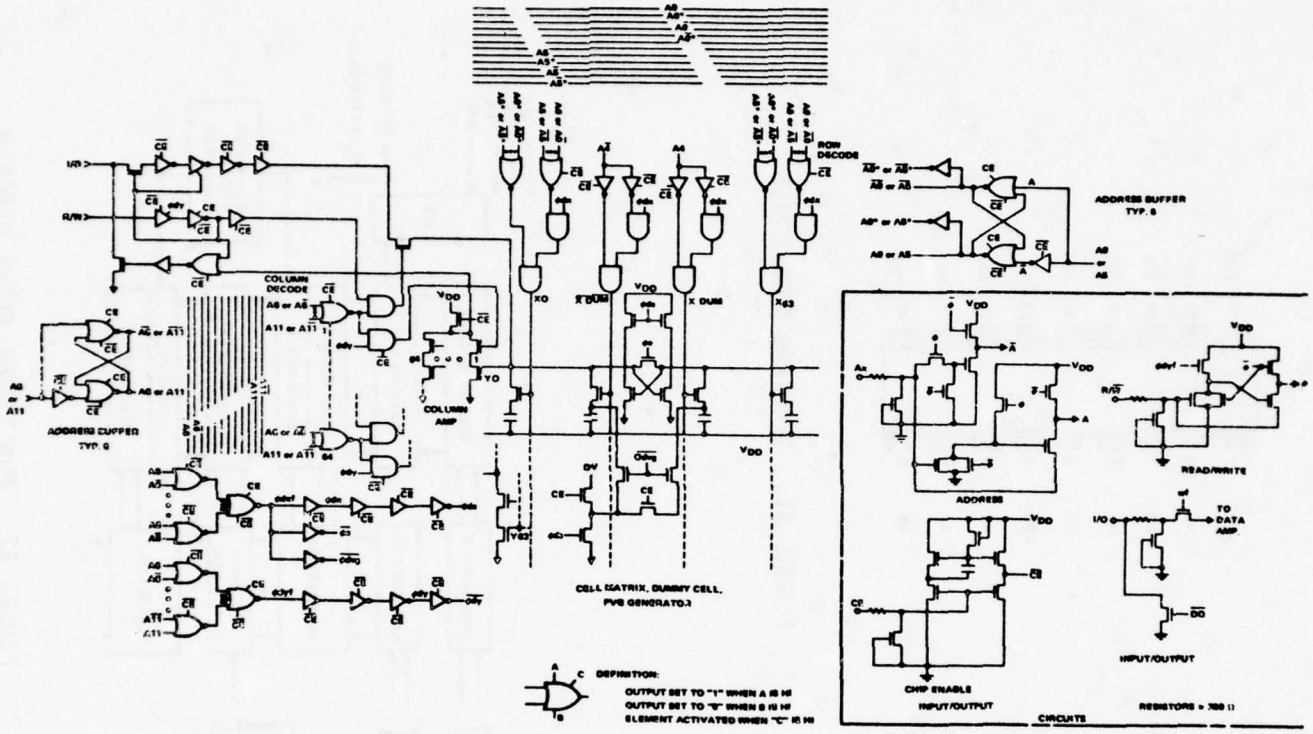


FIGURE A3. LOGIC DIAGRAM

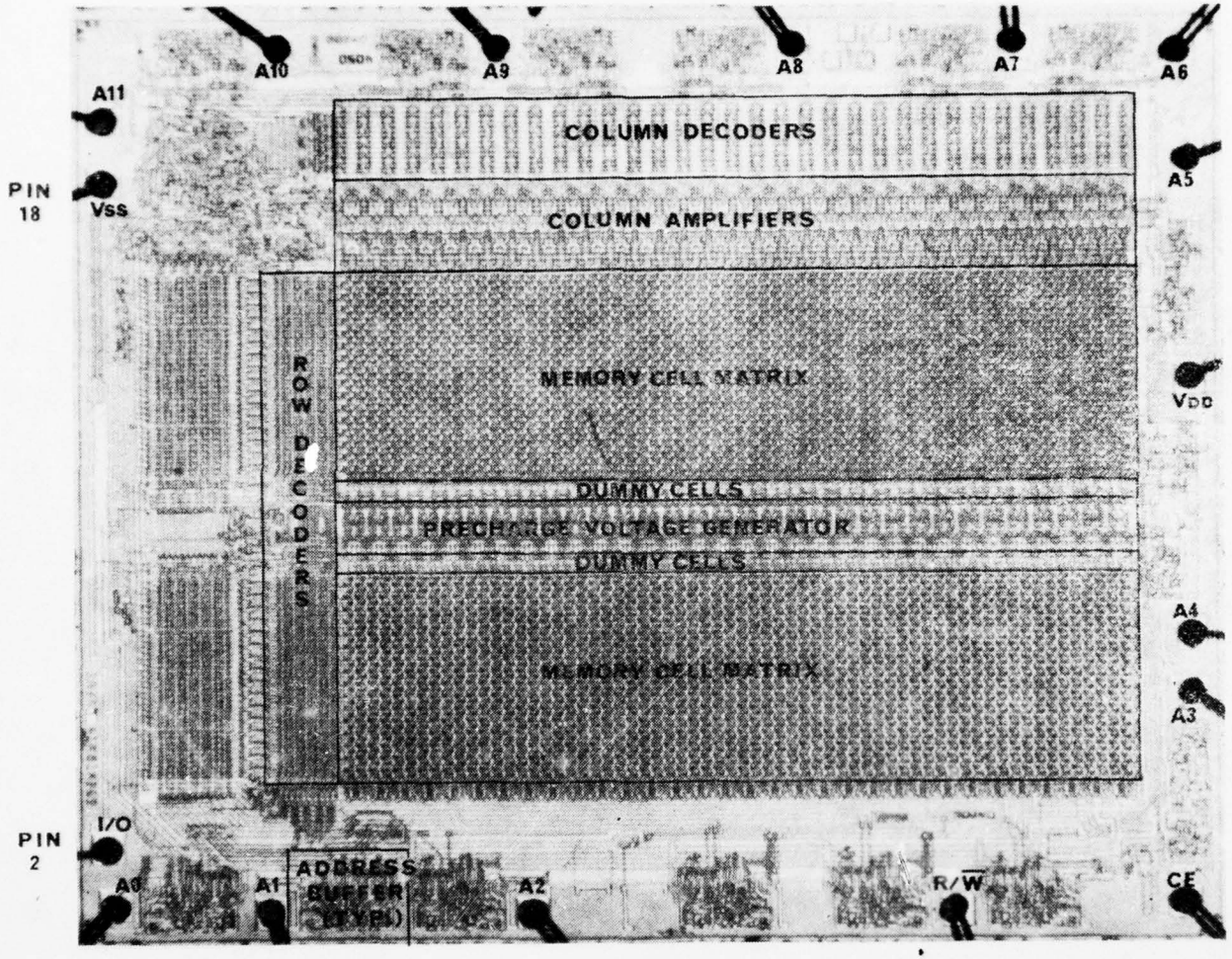
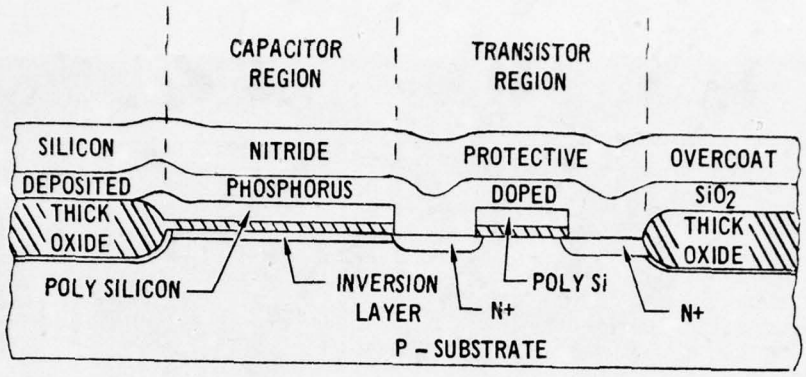
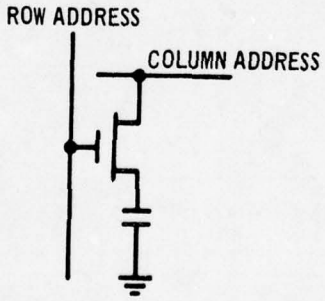


FIGURE A4. DIE PHOTOGRAPH



a) CROSS SECTION



b) SCHEMATIC

FIGURE A5. SINGLE TRANSISTOR CELL STRUCTURE

ROW ADDRESS: $A_4A_5A_1A_0A_2A_3$

COLUMN ADDRESS: $A_{11}A_{10}A_9A_8A_7A_6$

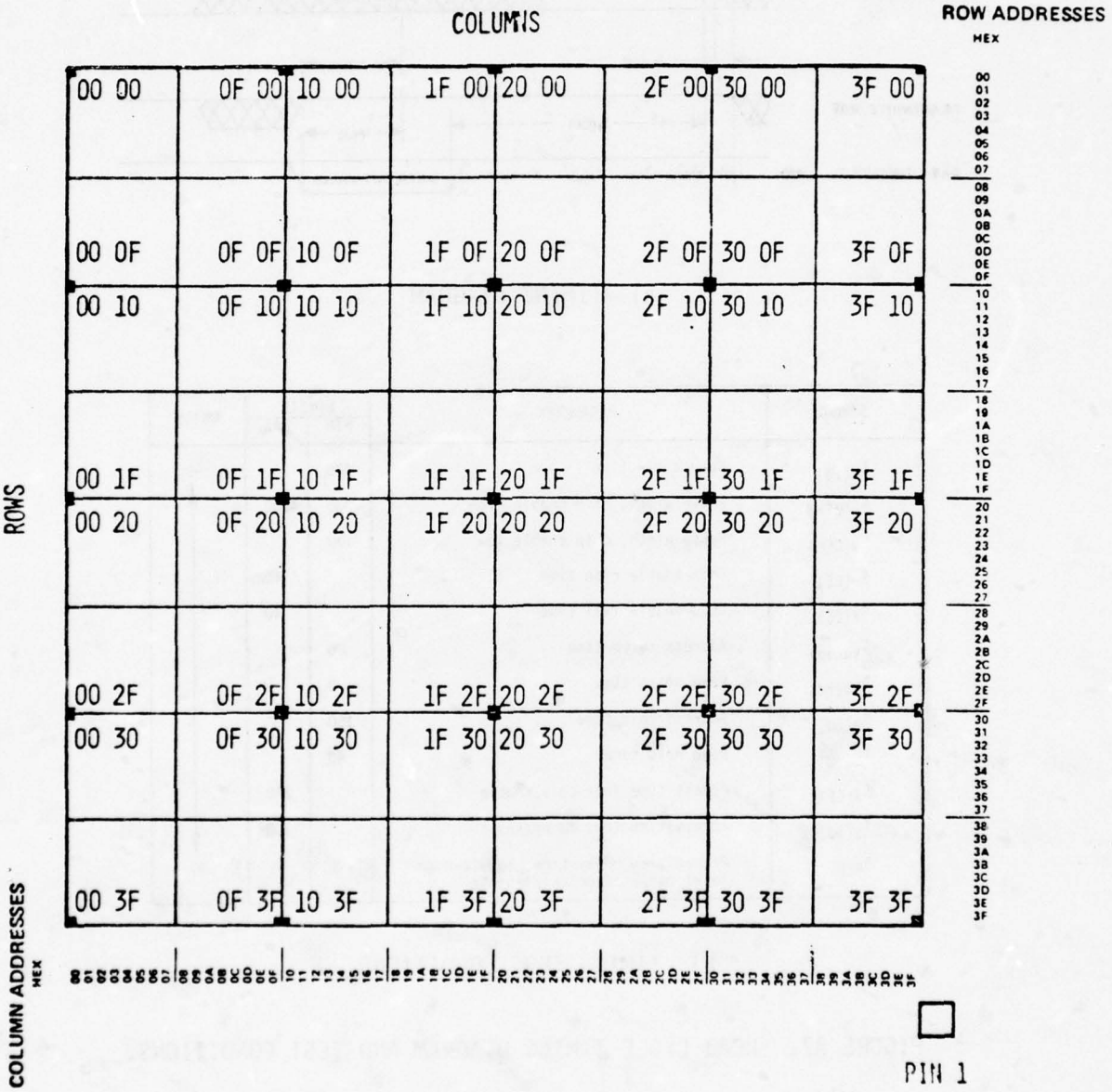
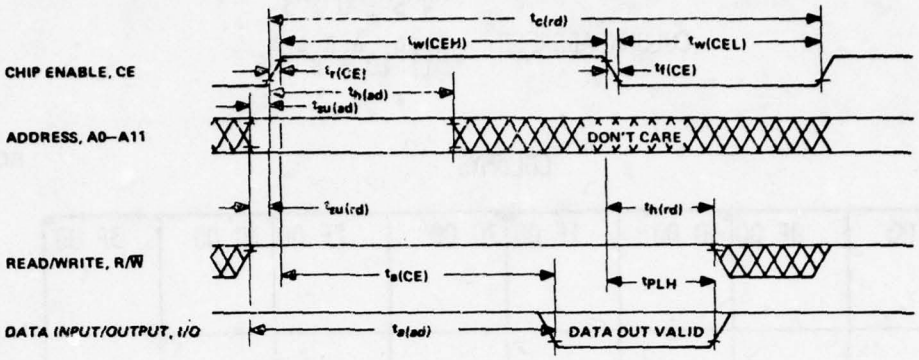


FIGURE A6. BIT MAP

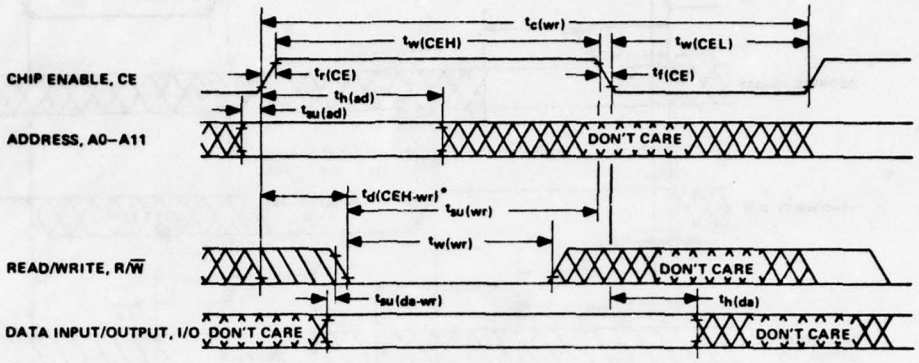


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
$t_{c(rd)}$	Read cycle time	470		nS
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	
$t_{w(CEL)}$	Pulse width, chip enable low	130		
$t_{r(CE)}$	Chip-enable rise time		40	
$t_{f(CE)}$	Chip-enable fall time		40	
$t_{su(ad)}$	Address setup time	0		
$t_{su(rd)}$	Read setup time	0		
$t_{h(ad)}$	Address hold time	150		
$t_{h(rd)}$	Read hold time	40		
$t_{a(CE)}$	Access time from chip enable		280	
$t_{a(ad)}$	Access time from addresses		300	
t_{PLH}	Propagation delay time, low-to-high level output from chip enable	40		nS

b) TIMING TEST CONDITIONS

FIGURE A7. READ CYCLE TIMING DIAGRAM AND TEST CONDITIONS.

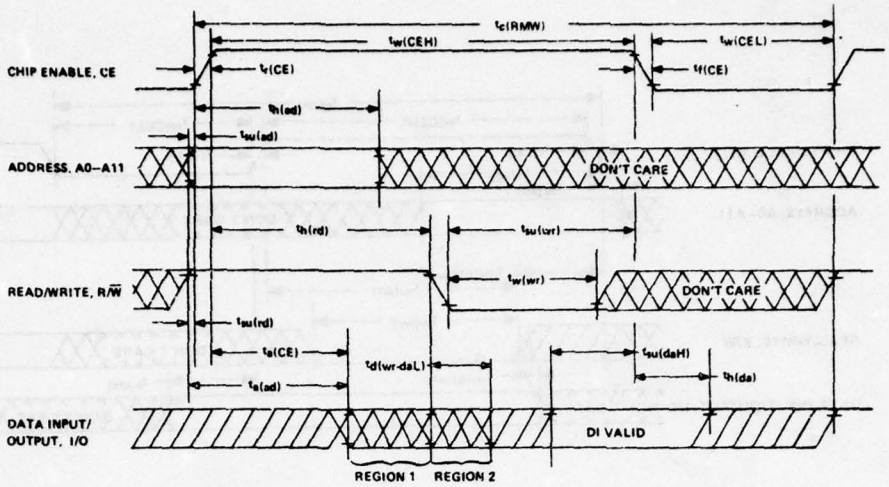


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
$t_{c(wr)}$	Write cycle time	470		nS
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	
$t_{w(CEL)}$	Pulse width, chip enable low	130		
$t_{w(wr)}$	Write pulse width	200		
$t_{r(CE)}$	Chip-enable rise time		40	
$t_{f(CE)}$	Chip-enable fall time		40	
$t_{su(ad)}$	Address setup time	0		
$t_{su(da-wr)}$	Data-to-write setup time	0		
$t_{su(wr)}$	Write-pulse setup time	240		
$t_{d(CEH-wr)}$	Chip-enable-high-to-write delay time		40	
$t_{h(ad)}$	Address hold time	150		
$t_{h(da)}$	Data hold time	40		nS

b) TIMING TEST CONDITIONS

FIGURE A8. WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS



REGION 1 – In region 1, data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is persmissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty.

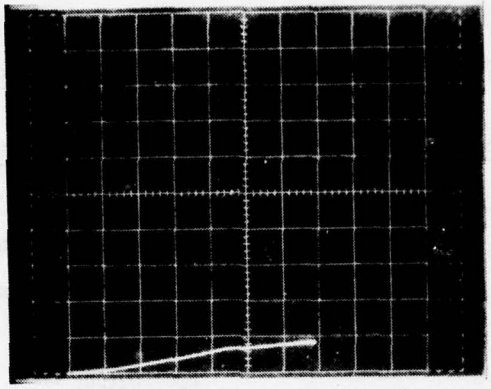
REGION 2 – In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be valid by the end of region 2.

a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
$t_{c(RMW)}$	Read, modify write cycle time	730		nS
$t_{w(CEH)}$	Pulse width, chip enable high	560	4000	
$t_{w(CEL)}$	Pulse width, chip enable low	130		
$t_{w(wr)}$	Write pulse width	200		
$t_{r(CE)}$	Chip-enable rise time		40	
$t_{f(CE)}$	Chip-enable fall time		40	
$t_{d(wr-daL)}$	Write to data-in-low delay time		20	
$t_{su(ad)}$	Address setup time	0		
$t_{su(daH)}$	Data-in-high setup time	240		
$t_{su(rd)}$	Read-pulse setup time	0		
$t_{su(wr)}$	Write-pulse setup time	240		
$t_{h(ad)}$	Address hold time	150		
$t_{h(rd)}$	Read hold time	300		
$t_{h(da)}$	Data hold time	40		nS

b) TIMING TEST CONDITIONS

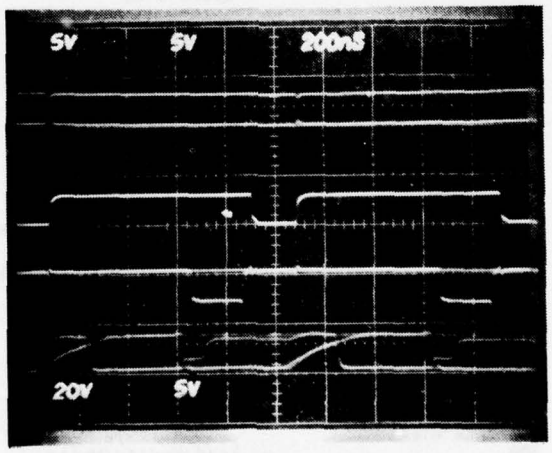
FIGURE A9. READ/MODIFY/WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS



I_{DD}
50 mA/DIV.

V_{DD} - 2 VOLTS/DIV.
$I_{DD\ (AVG)} \approx$ 40 mA AT V_{CC} = 12V

FIGURE A10. TYPICAL $I_{DD\ (AVG)}$ CURRENT FROM V_{DD} SUPPLY



$t_{A\ (ad)} \approx$ 160 nS AT V_{DD} = 11.4 VOLTS, V_{BB} = -5.5 VOLTS

FIGURE A11. TIMING WAVEFORMS FOR TYPICAL ADDRESS ACCESS TIME ($t_{a\ (ad)}$)

TABLE A1. SYMBOLS AND DEFINITIONS

SYMBOL	DEFINITION
V_{DD}	Supply voltage
V_{SS}	Common voltage node
V_{BB}	Supply voltage, substrate
CE	Chip enable
I/O	Input/Output
A0 thru A11 or ad	Address input
R/$\overline{W}$	Read or write input
I_{IL}	Low level input current
I_{IH}	High level input current
I_{DD}	Supply current from V_{DD} supply
I_{BB}	Supply current from V_{BB} supply
V_{OL}	Low level output voltage
V_{OH}	High level output voltage
t_c	Cycle time
t_a	Access time
V_{TH}	Threshold voltage
t_h	Hold time
t_w	Pulse width
CE-wr	CE high to write delay time
CE-dal	Chip enable to data low
da	data
rd	read
wr	write
RMW	Read/Modify/Write
t_{PLH}	Propagation delay time

TABLE A2. ALGORITHMS AND DESCRIPTIONS

ALGORITHM	DESCRIPTION
GALPAT	A. Write a background pattern of "0s" throughout memory. B. Write a "1" (test bit) at the first location. C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read in sequence until every location is read with test bit location. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell is used as test bit location.
GALWRT	A. Write a background pattern of "0s" throughout memory. B. Write a "1" into the background cell and read a "0" from the test bit cell. C. Repeat the sequence with the same test bit cell but the next background cell. Continue until entire memory is sequenced. D. Move test bit to next location and start sequence again. E. Repeat sequence until each cell is used as test bit location.
WALKING	A. Write a background pattern of "0s" throughout memory. B. Write a "1" at the first cell (test bit). C. Read the entire memory. D. Complement the "1" at the first cell and write a "1" into cell 2 (new test bit). E. Read the entire memory. F. Repeat the sequence until each cell is used as test bit location. G. Repeat steps B through F with a background pattern of "1s" throughout memory.
ROWPAT	A. Write a background pattern of "0s" for the first row. B. Write a "1" at the first location (test bit). C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read until all 64 locations in row is checked with the test bit. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell in the first row is used as test bit location. F. Increment until all rows are completed. G. Repeat steps B through F with a background pattern of "1s" throughout memory.

TABLE A2. ALGORITHMS AND DESCRIPTIONS (CONT.)

MARCH	A.	Write a background pattern of "0s" throughout memory.
	B.	Incrementing from address 0 to address 4095, read a "0" and write a "1" into each cell.
	C.	Incrementing from address 4095 to address 0, read an "1" and write an "0" into each cell.
	D.	Repeat steps B and C with a background pattern of "1s" throughout memory.
SHIFTING DIAGONAL	A.	Write a background of "0s" with a diagonal stripe of "1s".
	B.	Read the pattern incrementing the address by one each time.
	C.	Shift the stripe right one time.
	D.	Read out the pattern incrementing the address by one each time.
	E.	Repeat steps B through D until the stripe has been shifted 64 times and the pattern read out each time.
	F.	Repeat steps B through E with a background of "1s" with a diagonal stripe of "0s".
ADDCOMP	A.	Write an alternate pattern of "0s" and "1s" throughout memory.
	B.	Verify each location by the address sequence: address, address complement, address, address +1, etc.
	C.	Read out data pattern from memory.
REFRESH	A.	Write data (Alternating field of 1's and 0's) throughout memory.
	B.	Pause for the maximum specified refresh time.
	C.	Read out the pattern.
	D.	Write the complement pattern throughout memory.
	E.	Pause for the maximum specified refresh time.
	F.	Read out the complement pattern.

APPENDIX B

P/N AM9140

4096 BIT STATIC RANDOM ACCESS MEMORY

APPENDIX B

This appendix is included to supply various details of the Advanced Micro Devices AM9140. Figures B1 and B2 are the terminal layout and the functional block diagram of the device, respectively. The Figure B3 logic diagram, the Figure B4 die photograph, the Figure B5 cell schematic and topology, and the bit map shown in Figure B6 provide even greater layout and function detail. The timing requirements for the read, write, and read/modify/write cycles are provided in Figures B7, B8, and B9, respectively. Further electrical characteristics are shown in the Figure B10 and B11 photographs. Figure B10 is a curve tracer photograph of I_{CC} versus V_{CC} and Figure B11 shows several waveforms during a chip enable access time cycle.

In addition, two tables have been included in this appendix to supplement the discussion of this device in the report. Table B1 provides a list of the symbols and their definitions that are applicable to this device. Table B2 lists the algorithms used in this study of the AM9140.

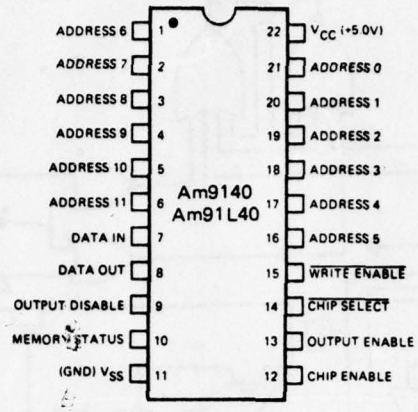


FIGURE B1. TERMINAL CONNECTION

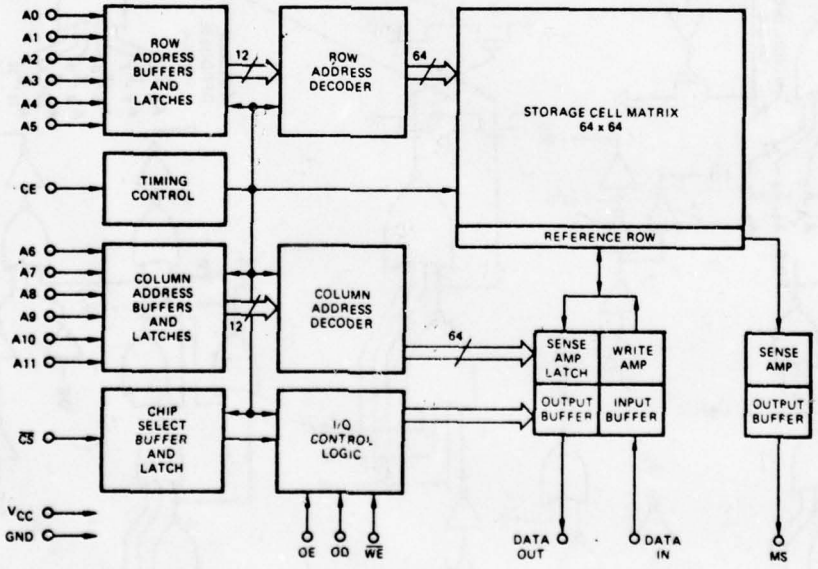


FIGURE B2. FUNCTIONAL BLOCK DIAGRAM

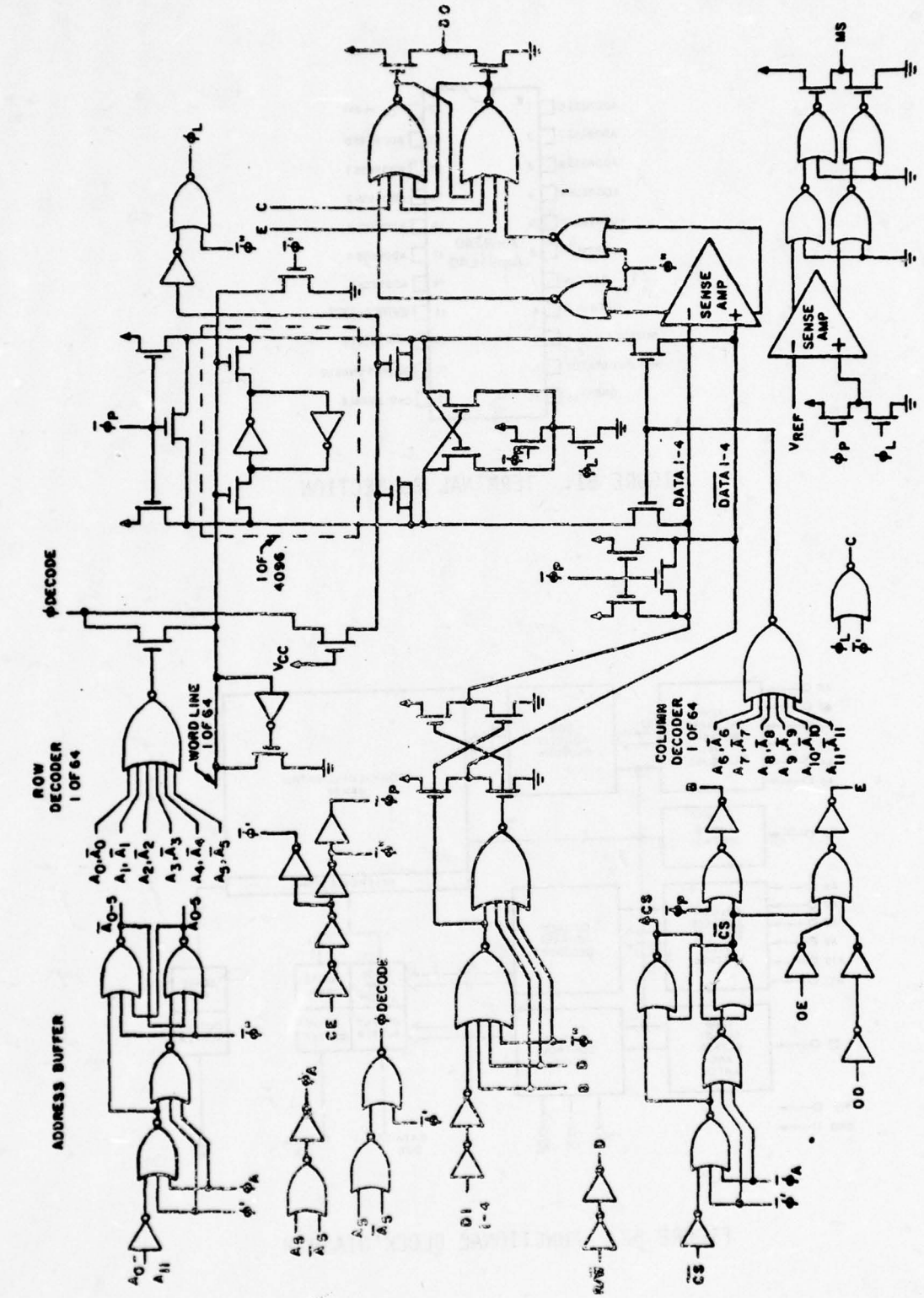


FIGURE B3. LOGIC DIAGRAM

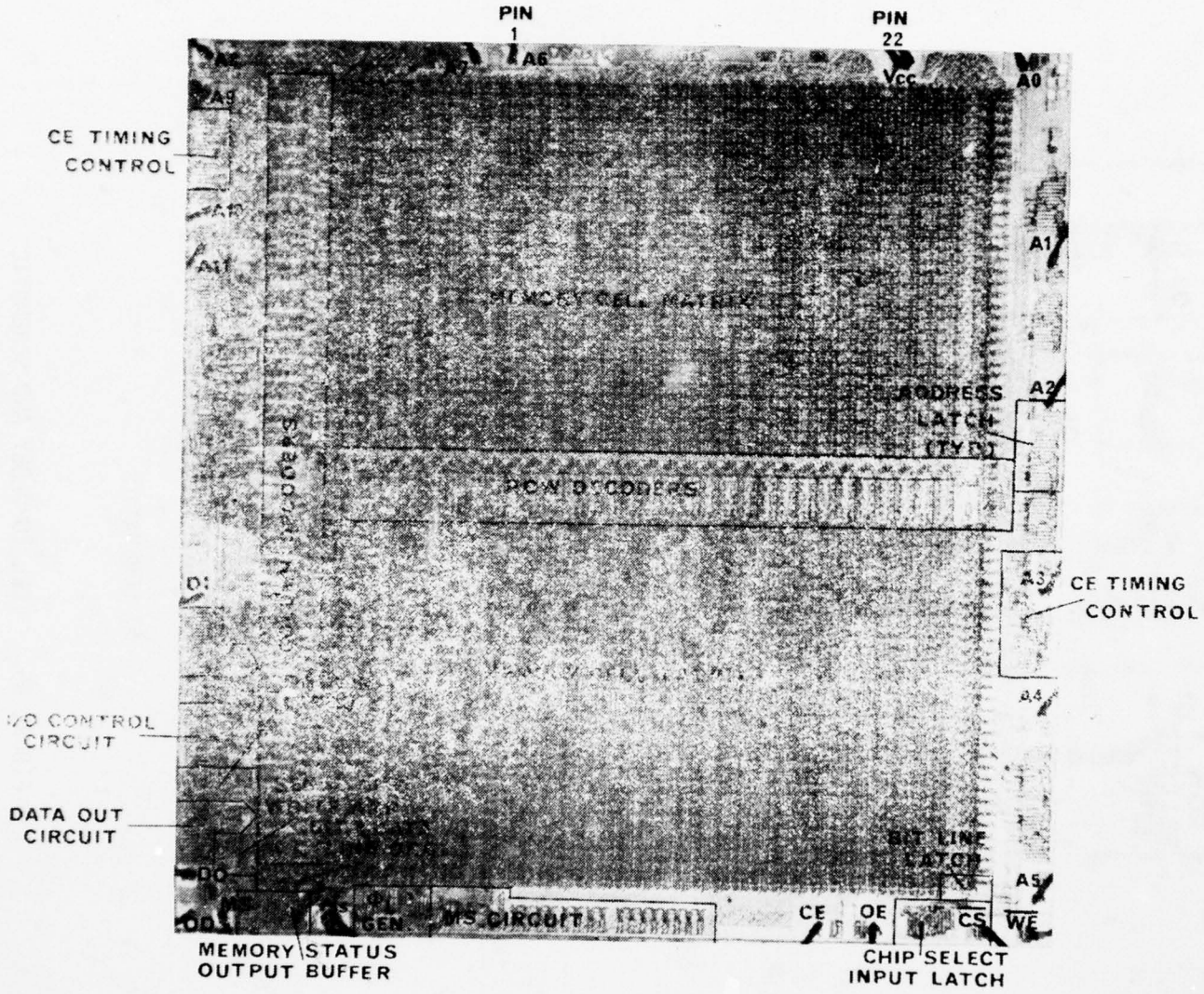
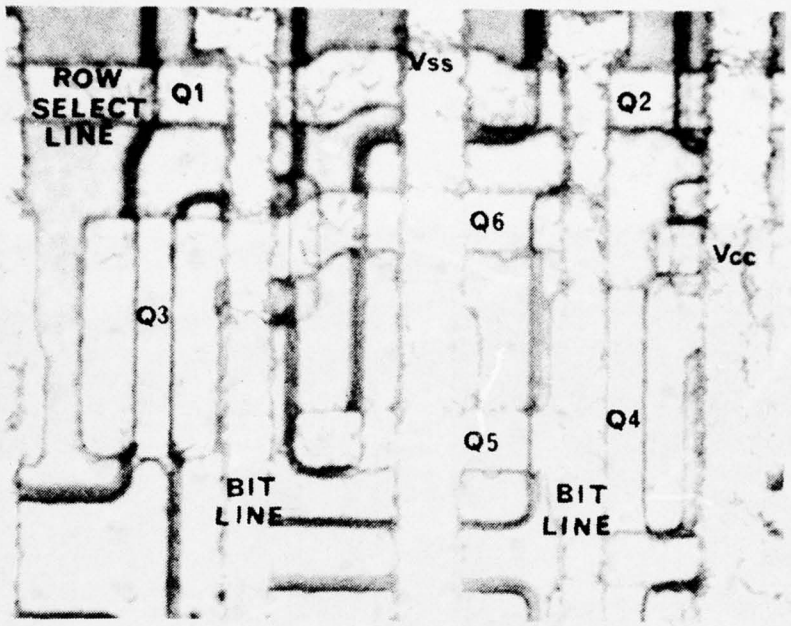
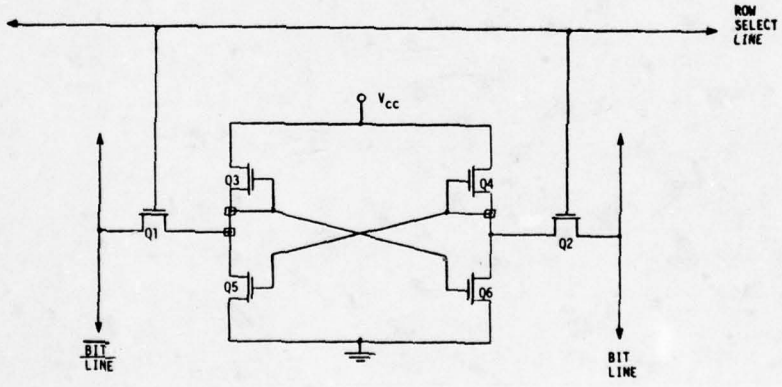


FIGURE B4. DIE PHOTOGRAPH



a) TOPOLOGY



b) SCHEMATIC

FIGURE B5. CELL TOPOLOGY AND SCHEMATIC

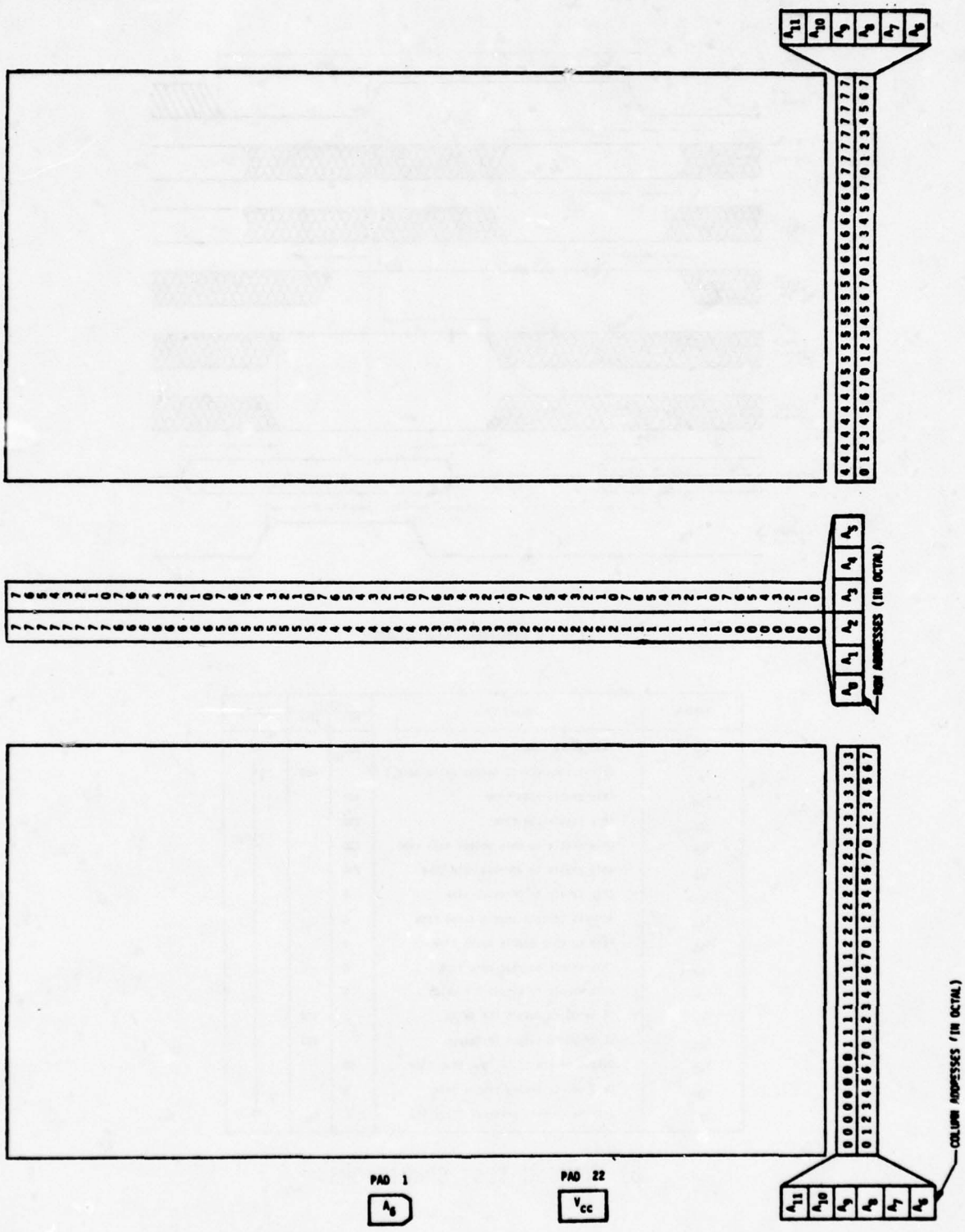
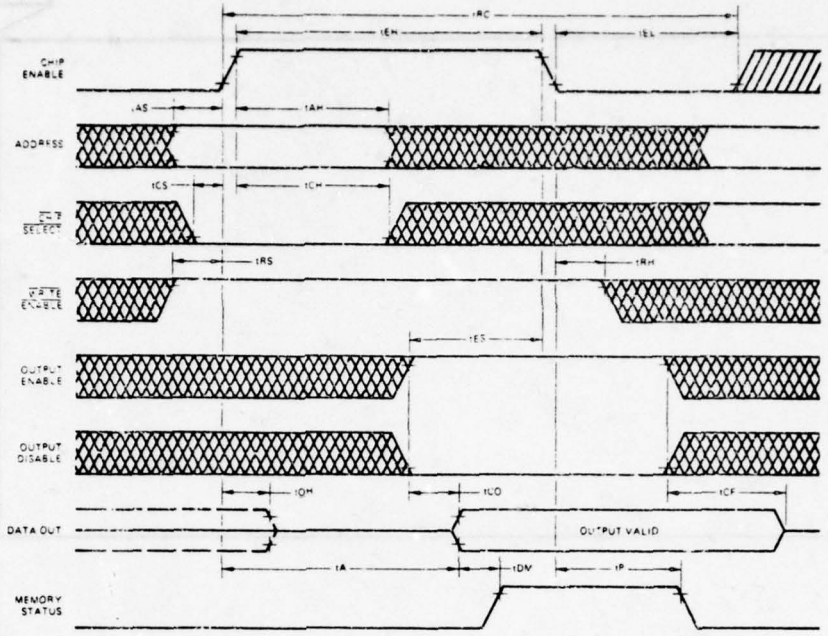


FIGURE B6. BIT MAP

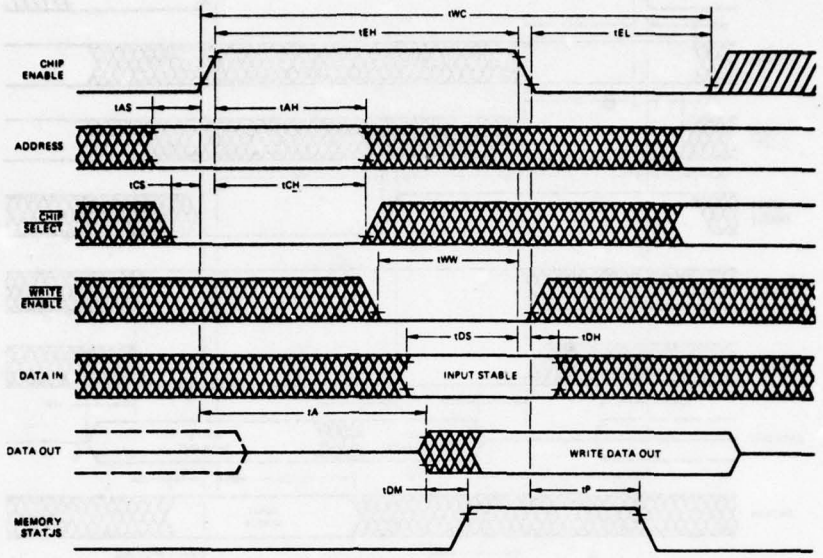


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
t_{RC}	Read cycle time	630		nS
t_A	Access time (CE to output valid delay)		400	
t_{EH}	Chip enable HIGH time	400		
t_{EL}	Chip enable LOW time	210		
t_{CH}	Chip enable to chip select hold time	200		
t_{AH}	Chip enable to address hold time	200		
t_{CS}	Chip select to CE setup time	-5		
t_{AS}	Address to chip enable setup time	0		
t_{RS}	Read to chip enable setup time	0		
t_{RH}	Chip enable to read hold time	0		
t_{OH}	Chip enable to output OFF delay	0		
t_{CF}	OE or OD to output OFF delay		120	
t_{CO}	OE or OD to output ON delay		220	
t_{ES}	Output enable to CE low setup time	90		
t_{DM}	Data out to memory status delay	0		
t_P	Internal preset interval (Note 14)		t_{EL}	nS

b) TIMING TEST CONDITIONS

FIGURE 87. READ CYCLE TIMING DIAGRAM AND TEST CONDITIONS

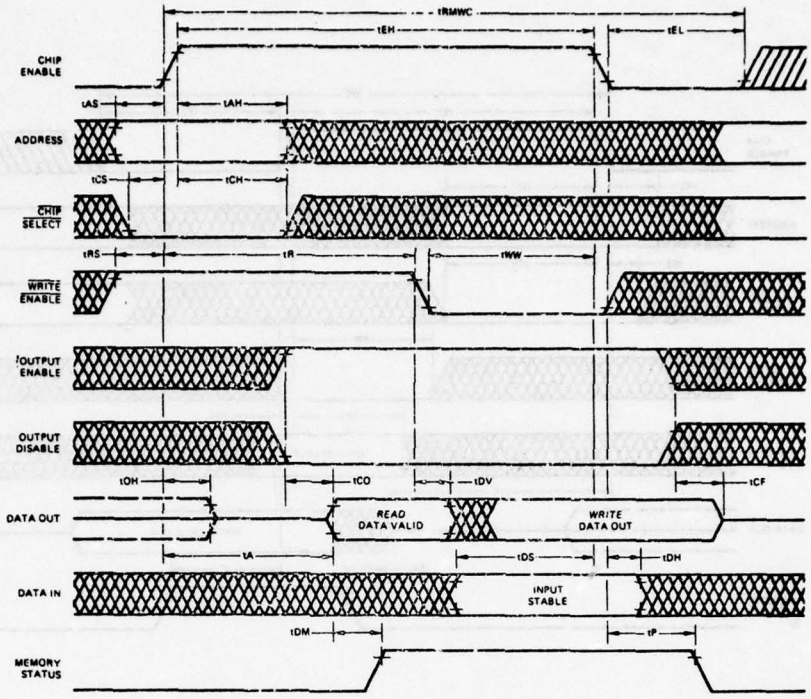


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
t_{WC}	Write cycle time	630		nS
t_A	Access time (CE to output ON delay)		400	
t_{EH}	Chip enable HIGH time	400		
t_{EL}	Chip enable LOW time	210		
t_{AS}	Address to chip enable setup time	0		
t_{AH}	Chip enable to address hold time	200		
t_{CS}	Chip select to CE setup time	-5		
t_{CH}	Chip enable to chip select hold time	200		
t_{WW}	Write pulse width	200		
t_{DS}	Data input setup time	80		
t_{DH}	Data input hold time	0		
t_{DM}	Data out to memory status delay	0		
t_p	Internal preset inverval		t_{EL}	nS

b) TIMING TEST CONDITIONS

FIGURE B8. WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS

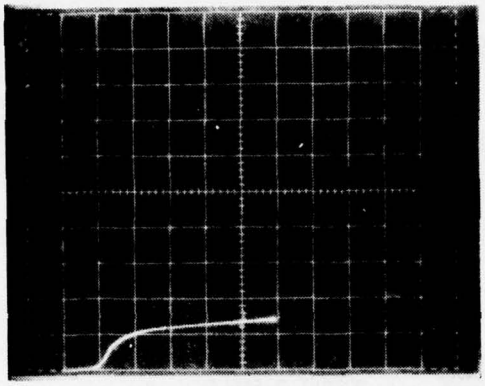


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
t_{RMWC}	R/M/W cycle time	970		nS
t_A	Access time (CE to output valid delay)		400	
t_{EH}	Chip enable HIGH time	700		
t_{EL}	Chip enable LOW time	250		
t_{CH}	Chip enable to chip select hold time	200		
t_{AH}	Chip enable to address hold time	200		
t_{CS}	Chip select to CE setup time	-5		
t_{AS}	Address to chip enable setup time	0		
t_{RS}	Read to chip enable setup time	0		
t_{OH}	Chip enable to output OFF delay	0		
t_{DH}	Data input hold time	0		
t_{DS}	Data input setup time	80		
t_{WW}	Write pulse width	200		
t_{CF}	OE or OD to output OFF delay		120	
t_{CO}	OE or OD to output ON delay		220	
t_{DV}	Data valid after write delay	10		
t_R	Read mode hold time	t_A		
t_{DM}	Data out to memory status delay	0		
t_P	Internal preset interval		t_{EL}	nS

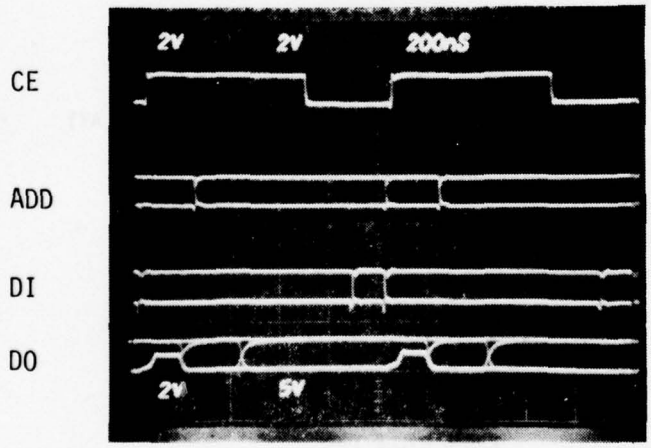
b) TIMING TEST CONDITIONS

FIGURE B9. READ/MODIFY/WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS



V_{CC} - 1.0 VOLTS/DIV.
$I_{CC} \approx 68$ mA AT V_{DD} = 5V

FIGURE B10. TYPICAL I_{CC} CURRENT FROM V_{CC} SUPPLY



$t_A \approx 160$ nS AT V_{DD} = 4.5 VOLTS

FIGURE B11. TIMING WAVEFORMS FOR TYPICAL CHIP ENABLE ACCESS TIME (t_A)

TABLE B1. SYMBOLS AND DEFINITIONS

SYMBOL	DEFINITION
V_{CC}	SUPPLY VOLTAGE
V_{SS}	COMMON VOLTAGE NODE
CE	CHIP ENABLE INPUT
CS	CHIP SELECT INPUT
WE	WRITE ENABLE INPUT
OE	OUTPUT ENABLE
OD	OUTPUT DISABLE
DI	DATA INPUT
DO	DATA OUTPUT
MS	MEMORY STATUS OUTPUT
A0 THRU A11	ADDRESS INPUT
I_{IH}	HIGH LEVEL INPUT CURRENT
I_{OHZ}	HIGH IMPEDANCE STATE, HIGH LEVEL OUTPUT CURRENT
I_{OLZ}	HIGH IMPEDANCE STATE, LOW LEVEL OUTPUT CURRENT
I_{CC}	SUPPLY CURRENT FROM V_{CC} SUPPLY
V_{OH}	HIGH LEVEL OUTPUT VOLTAGE
V_{OL}	LOW LEVEL OUTPUT VOLTAGE
V_{IH}	HIGH LEVEL INPUT VOLTAGE
V_{IL}	LOW LEVEL INPUT VOLTAGE
t_{RC}	READ CYCLE TIME
t_A	ACCESS TIME (CE TO OUTPUT VALID DELAY)
t_{CF}	OE/OD TO OUTPUT OFF DELAY
t_{CO}	OE/OD TO OUTPUT ON DELAY
t_{DM}	DATA OUT TO MEMORY STATUS DELAY
t_p	INTERNAL PRESET INTERVAL
t_{WC}	WRITE CYCLE
t_{WW}	WRITE PULSE WIDTH
t_{DS}	INPUT DATA SETUP TIME
t_{DH}	INPUT DATA HOLD TIME
t_{RMWC}	R/M/W CYCLE TIME
t_{DV}	DATA VALID AFTER WRITE DELAY
t_{EH}	CHIP ENABLE HIGH TIME
t_{EL}	CHIP ENABLE LOW TIME

TABLE B2. ALGORITHMS AND DESCRIPTIONS

ALGORITHM	DESCRIPTION
GALPAT	A. Write a background pattern of "Os" throughout memory. B. Write a "1" (test bit) at the first location. C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read in sequence until every location is read with test bit location. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell is used as test bit location.
GALWRT	A. Write a background pattern of "Os" throughout memory. B. Write a "1" into the background cell and read a "0" from the test bit cell. C. Repeat the sequence with the same test bit cell but the next background cell. Continue until entire memory is sequenced. D. Move test bit to next location and start sequence again. E. Repeat sequence until each cell is used as test bit location.
WALKING	A. Write a background pattern of "Os" throughout memory. B. Write a "1" at the first cell (test bit). C. Read the entire memory. D. Complement the "1" at the first cell and write a "1" into cell 2 (new test bit). E. Read the entire memory. F. Repeat the sequence until each cell is used as test bit location. G. Repeat steps B through F with a background pattern of "1s" throughout memory.
ROWPAT	A. Write a background pattern of "Os" for the first row. B. Write a "1" at the first location (test bit). C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read until all 64 locations in row is checked with the test bit. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell in the first row is used as test bit location. F. Increment until all rows are completed. G. Repeat steps B through F with a background pattern of "1s" throughout memory.

TABLE B2. ALGORITHMS AND DESCRIPTIONS (CONT.)

MARCH	A. Write a background pattern of "0s" throughout memory. B. Incrementing from address 0 to address 4095, read a "0" and write a "1" into each cell. C. Incrementing from address 4095 to address 0, read an "1" and write an "0" into each cell. D. Repeat steps B and C with a background pattern of "1s" throughout memory.
SHIFTING DIAGONAL	A. Write a background of "0s" with a diagonal stripe of "1s". B. Read the pattern incrementing the address by one each time. C. Shift the stripe right one time. D. Read out the pattern incrementing the address by one each time. E. Repeat steps B through D until the stripe has been shifted 64 times and the pattern read out each time. F. Repeat steps B through E with a background of "1s" with a diagonal stripe of "0s".
ADDCOMP	A. Write an alternate pattern of "0s" and "1s" throughout memory. B. Verify each location by the address sequence: address, address complement, address, address + 1, etc. C. Read out data pattern from memory.

APPENDIX C

P/N MWS5501

1024 BIT STATIC RANDOM ACCESS MEMORY

APPENDIX C

This appendix is included to supply various details of the RCA MWS5501. Figures C1 and C2 are the terminal layout and the functional block diagram of the device, respectively. The Figure C3 logic diagram, the Figure C4 die photograph, the Figure C5 cell structure and partial cross section, and the bit map shown in Figure C6 provide even greater layout and function detail. The timing requirements for the read, write, and read/modify/write cycles are provided in Figures C7, C8, and C9, respectively. Further electrical characteristics are shown in the Figure C10, C11 and C12 photographs. Figure C10 is a curve tracer photograph of I_{DD} versus V_{DD} and Figures C11 and C12 show several waveforms during a read access time cycle with different V_{DD} voltages.

In addition, two tables have been included in this appendix to supplement the discussion of this device in the report. Table C1 provides a list of the symbols and their definitions that are applicable to this device. Table C2 lists the algorithms used in this study of the MWS5501.

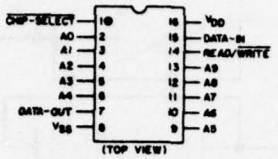


FIGURE C1. TERMINAL CONNECTION

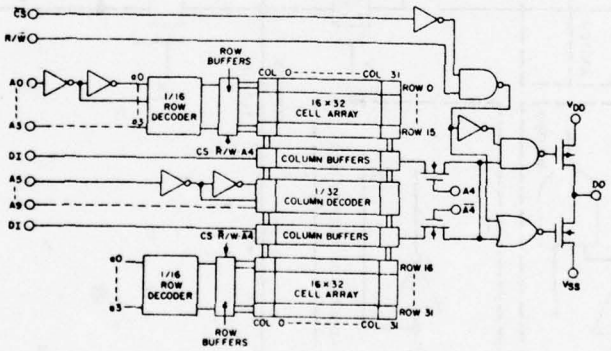


FIGURE C2. FUNCTIONAL BLOCK DIAGRAM

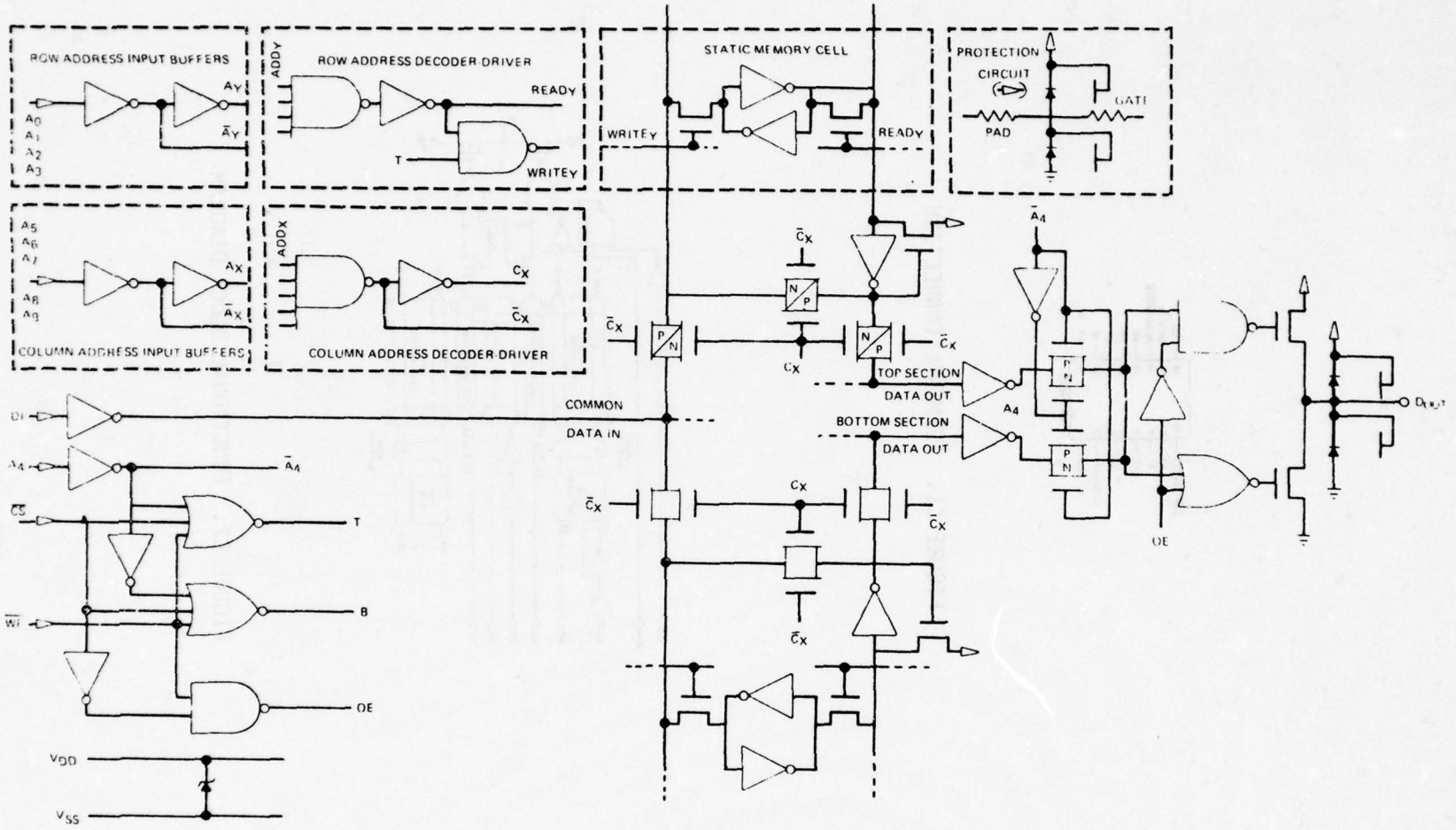


FIGURE C3. LOGIC DIAGRAM

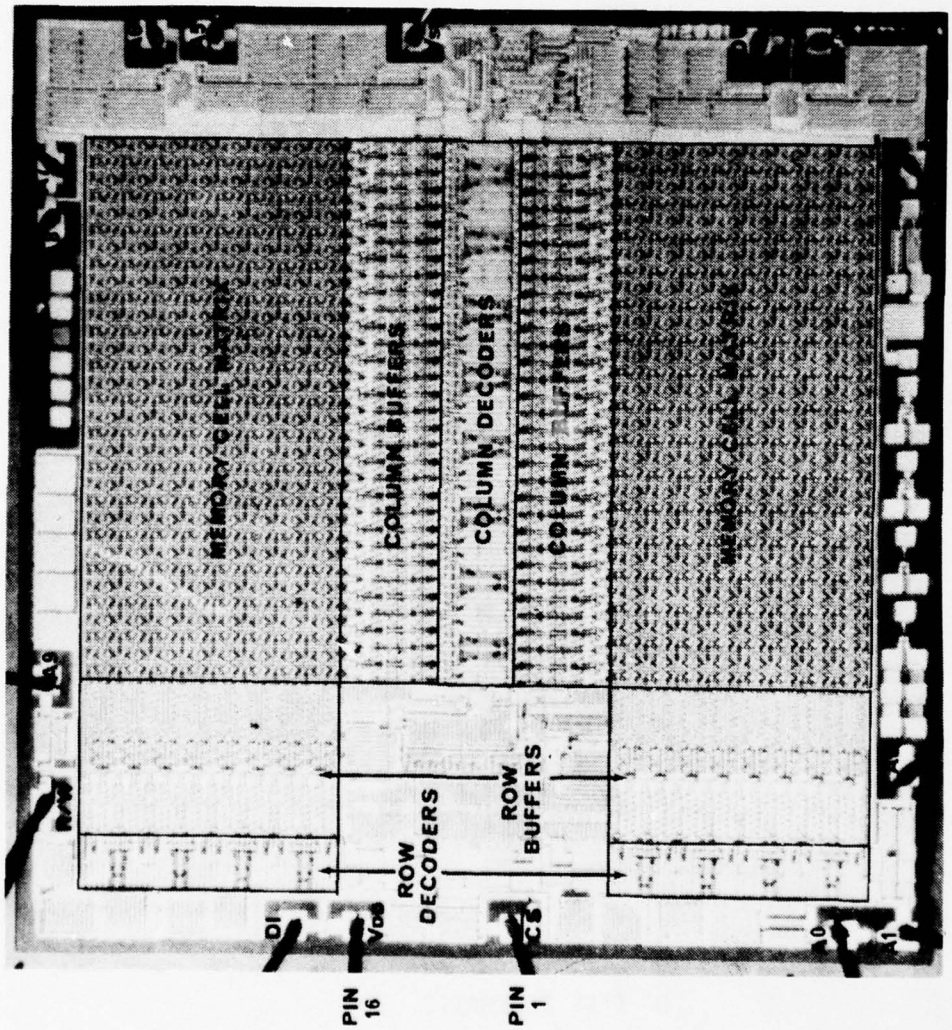
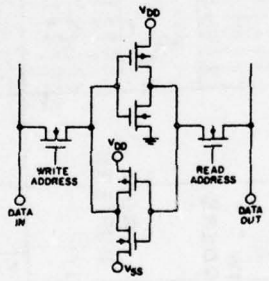


FIGURE C4. DIE PHOTOGRAPH

LEVEL	LEGEND
SOS epitaxy	
Channel oxide	
Polycrystalline silicon	
Phosphorus-doped glass	
Boron-doped glass	
Aluminum	

A) CROSS SECTION OF TRANSISTOR PAIR



B) CELL SCHEMATIC

FIGURE C5. CELL STRUCTURE AND PARTIAL CROSS SECTION

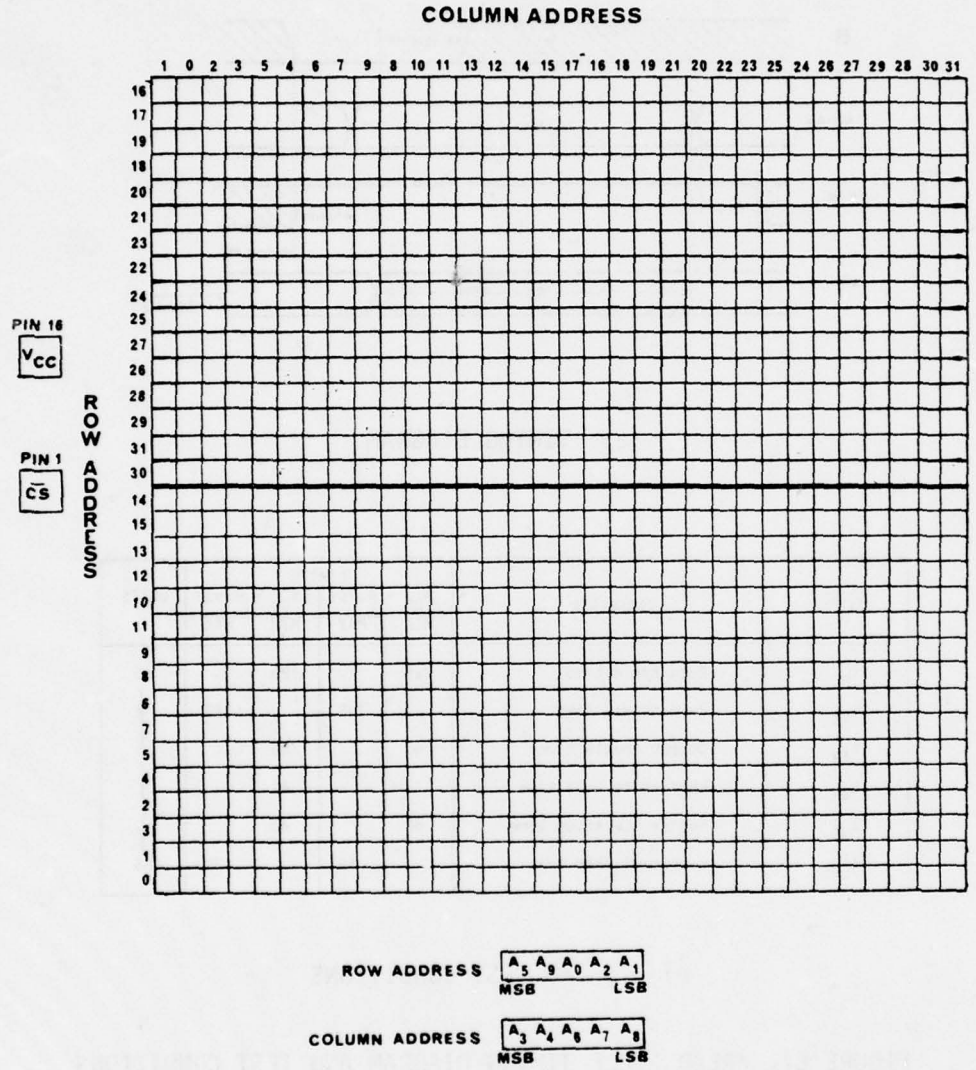
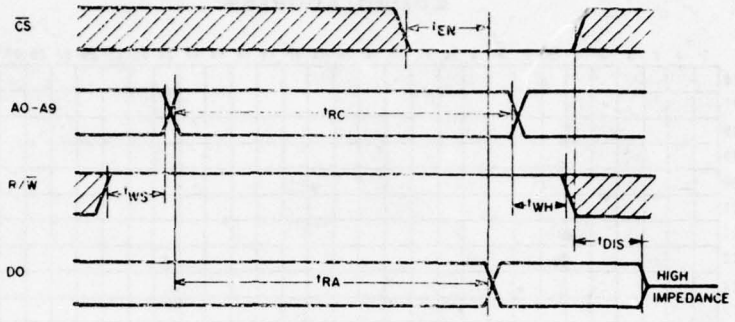


FIGURE C6. BIT MAP

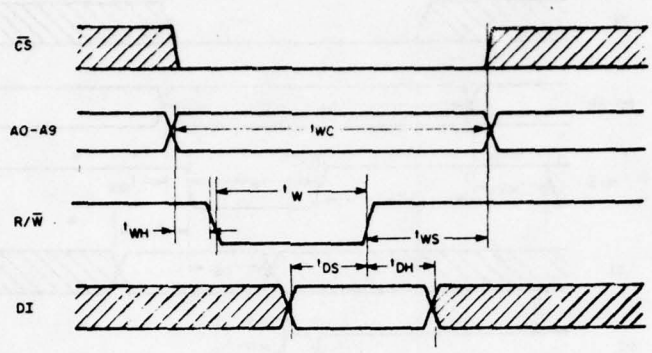


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS V_{DD} = 4.75V MIN	LIMITS V_{DD} = 4.75V MAX	LIMITS V_{DD} = 9.50V MIN	LIMITS V_{DD} = 9.50V MAX	UNITS
t_{RC}	Read cycle time	225		120		nS
t_{RA}	Read access time		225		120	
t_{EN}	Output enable time	60		40		
t_{WH}	Read/write hold time	70		40		
t_{WS}	Read/write setup time	60		40		
t_{DIS}	Output disable time		60		30	nS

b) TIMING TEST CONDITIONS

FIGURE C7. READ CYCLE TIMING DIAGRAM AND TEST CONDITIONS

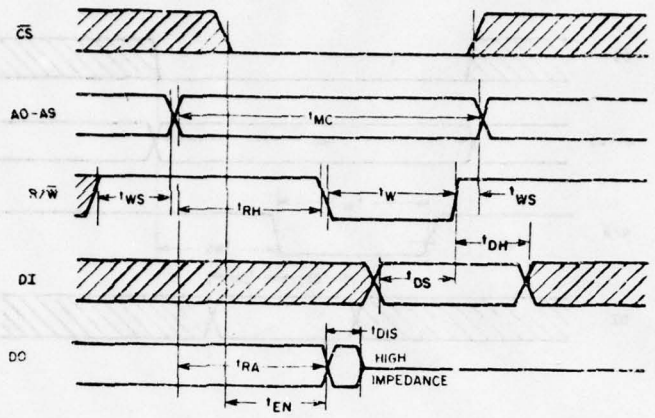


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS V_{DD} = 4.75V MIN	LIMITS V_{DD} = 4.75V MAX	LIMITS V_{DD} = 9.50V MIN	LIMITS V_{DD} = 9.50V MAX	UNITS
t_{WC}	Write cycle time	225		120		nS
t_W	Write pulse width	115		80		
t_{WH}	Read/write hold time	70		40		
t_{WS}	Read/write setup time	60		40		
t_{DS}	Data setup time	45		30		
t_{DH}	Data hold time	30		30		nS

b) TIMING TEST CONDITIONS

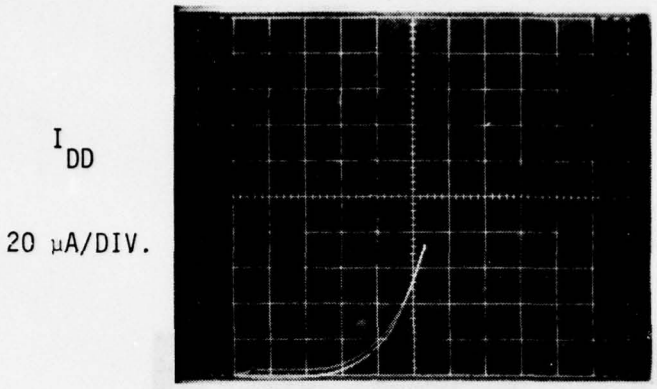
FIGURE C8. WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS



a) TIMING DIAGRAM

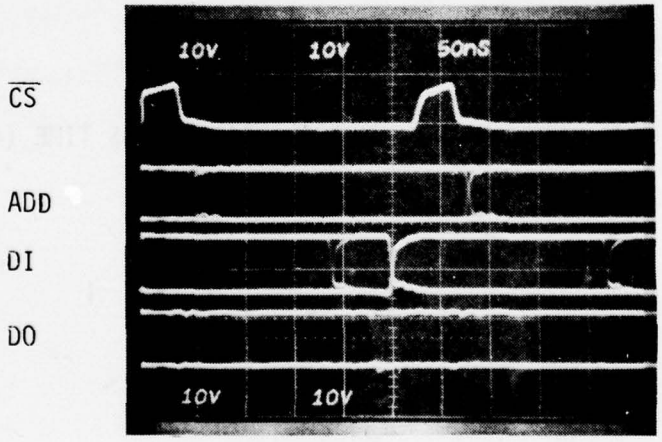
SYMBOL	PARAMETER	LIMITS				UNITS
		V_{DD} = 4.75V		V_{DD} = 9.50V		
		MIN	MAX	MIN	MAX	
t_{MC}	R/M/W cycle time	400		210		nS
t_{RA}	Read access time		225		120	
t_{RH}	Read hold time	225		120		
t_{EN}	Output enable time	60		40		
t_{W}	Write pulse width	115		80		
t_{WS}	Read/write setup time	60		40		
t_{DS}	Data setup time	45		30		
t_{DH}	Data hold time	30		30		
t_{DIS}	Output disable time		60		30	nS

FIGURE C9. READ/MODIFY/WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS



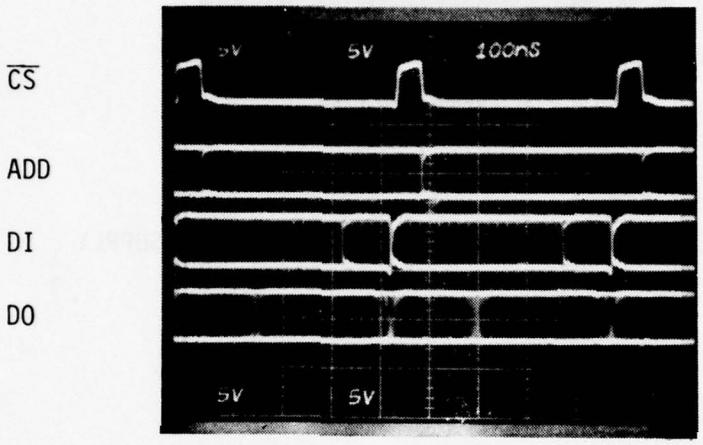
V_{DD} - 2 VOLTS/DIV.
$I_{DD} \approx 50$ μA AT V_{DD} = 10V

FIGURE C10. TYPICAL I_{DD} CURRENT FROM V_{DD} SUPPLY



$t_{RA} \approx 70$ nS AT V_{DD} = 10.5 VOLTS

FIGURE C11. TIMING WAVEFORMS FOR TYPICAL READ ACCESS TIME (t_{RA})



$t_{RA} \approx 140$ nS AT $V_{DD} = 4.75$ VOLTS

FIGURE C12. TIMING WAVEFORMS FOR TYPICAL READ ACCESS TIME (t_{RA})

TABLE C1. SYMBOLS AND DEFINITIONS

SYMBOL	DEFINITION
V_{DD}	SUPPLY VOLTAGE
V_{SS}	COMMON VOLTAGE NODE
$\overline{CS}$	CHIP SELECT
DI	DATA IN
DO	DATA OUT
AO THRU A9	ADDRESS INPUT
R/$\overline{W}$	READ OR WRITE INPUT
$V_{IC(POS)}$	INPUT CLAMP VOLTAGE, POSITIVE
$V_{IC(NEG)}$	INPUT CLAMP VOLTAGE, NEGATIVE
V_{OH}	HIGH LEVEL OUTPUT VOLTAGE
V_{OL}	LOW LEVEL OUTPUT VOLTAGE
I_{IH}	HIGH LEVEL INPUT CURRENT
I_{IL}	LOW LEVEL INPUT CURRENT
I_{DD}	SUPPLY CURRENT FROM V_{DD} SUPPLY
V_{THN}	THRESHOLD VOLTAGE
V_{THP}	THRESHOLD VOLTAGE
t_{RC}	READ CYCLE TIME
t_{WC}	WRITE CYCLE TIME
t_{MC}	READ/MODIFY/WRITE CYCLE TIME
t_{RA}	READ ACCESS TIME
t_{EN}	OUTPUT ENABLE TIME
t_{DIS}	OUTPUT DISABLE TIME
t_{W}	WRITE PULSE WIDTH
t_{DS}	INPUT DATA SETUP TIME
t_{DH}	INPUT DATA HOLD TIME

TABLE C2. ALGORITHMS AND DESCRIPTIONS

ALGORITHM	DESCRIPTION
GALPAT	A. Write a background pattern of "0s" throughout memory. B. Write a "1" (test bit) at the first location. C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read in sequence until every location is read with test bit location. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell is used as test bit location. F. Repeat steps B through E with a background pattern of "1s" throughout memory.
GALWRT	A. Write a background pattern of "0s" throughout memory. B. Write a "1" into the background cell and read a "0" from the test bit cell. C. Repeat the sequence with the same test bit cell but the next background cell. Continue until entire memory is sequenced. D. Move test bit to next location and start sequence again. E. Repeat sequence until each cell is used as test bit location. F. Repeat steps B through E with a background pattern of "1s" throughout memory.
WALKING	A. Write a background pattern of "0s" throughout memory. B. Write a "1" at the first cell (test bit). C. Read the entire memory. D. Complement the "1" at the first cell and write a "1" into cell 2 (new test bit). E. Read the entire memory. F. Repeat the sequence until each cell is used as test bit location. G. Repeat steps B through F with a background pattern of "1s" throughout memory.
ROWPAT	A. Write a background pattern of "0s" for the first row. B. Write a "1" at the first location (test bit). C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read until all 32 locations in row is checked with the test bit. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell in the first row is used as test bit location. F. Increment until all rows are completed. G. Repeat steps B through F with a background pattern of "1s" throughout memory.

TABLE C2. ALGORITHMS AND DESCRIPTIONS (CONT.)

MARCH	A. Write a background pattern of "0s" throughout memory. B. Incrementing from address 0 to address 1023 read a "0" and write a "1" into each cell. C. Incrementing from address 1023 to address 0, read an "1" and write an "0" into each cell. D. Repeat steps B and C with a background pattern of "1s" throughout memory.
SHIFTING DIAGONAL	A. Write a background of "0s" with a diagonal stripe of "1s". B. Read the pattern incrementing the address by one each time. C. Shift the stripe right one time. D. Read out the pattern incrementing the address by one each time. E. Repeat steps B through D until the stripe has been shifted 32 times and the pattern read out each time. F. Repeat steps B through E with a background of "1s" with a diagonal stripe of "0s".
ADDCOMP	A. Write an alternate pattern of "0s" and "1s" throughout memory. B. Verify each location by the address sequence: address, address complement, address, address + 1, etc. C. Read out data pattern from memory.

APPENDIX D

P/N 93481

4096 BIT DYNAMIC RANDOM ACCESS MEMORY

APPENDIX D

This appendix is included to supply various details of the Fairchild 93481. Figures D1 and D2 are the terminal layout and the functional block diagram of the device, respectively. The Figure D3 die photograph, the Figure D4 transistor cell structure and the bit map shown in Figure D5 provide even greater layout and function detail. The timing requirements for the read, write, and read/modify/write cycles are provided in Figures D6, D7, and D8, respectively. Further electrical characteristics are shown in the Figure D9 and D10 photographs. Figure D9 is a curve tracer photograph of I_{CC} versus V_{CC} and Figure D10 shows several waveforms during a column address access time cycle.

In addition, two tables have been included in this appendix to supplement the discussion of this device in the report. Table D1 provides a list of the symbols and their definitions that are applicable to this device. Table D2 lists the algorithms used in this study of the 93481.

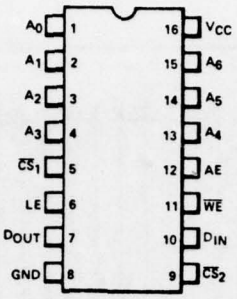


FIGURE D1. TERMINAL CONNECTION

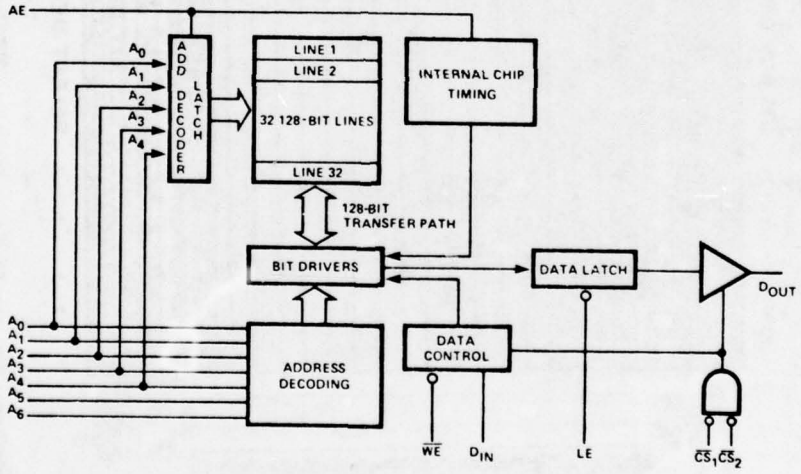


FIGURE D2. FUNCTIONAL BLOCK DIAGRAM

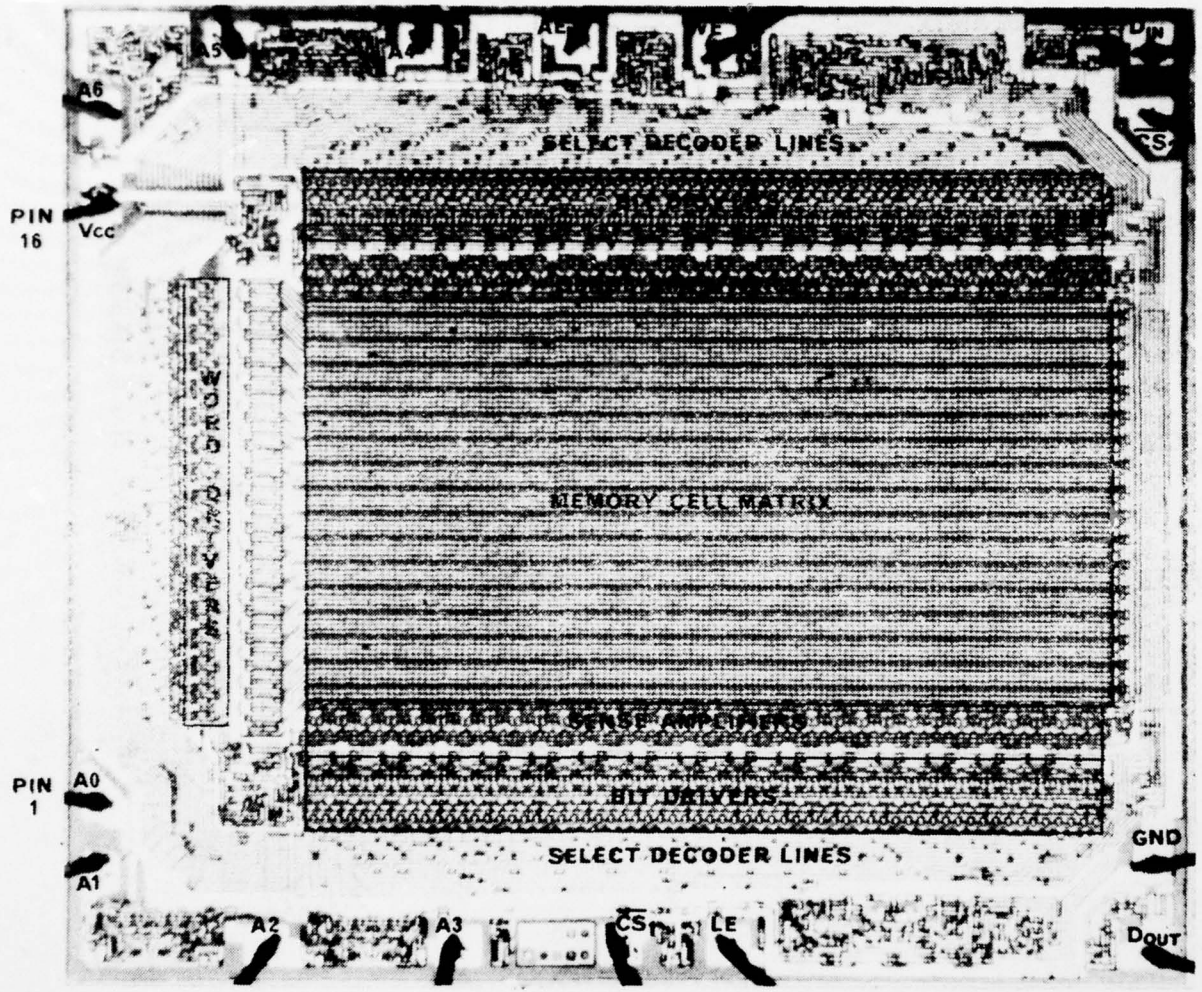
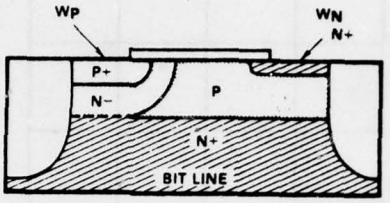
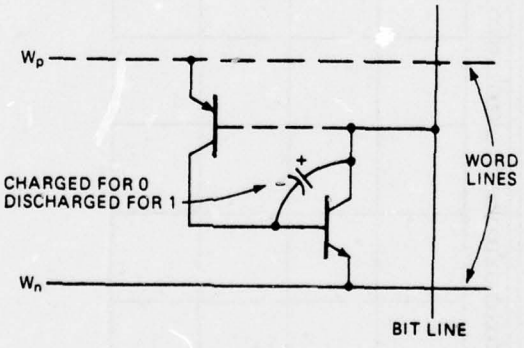


FIGURE D3. DIE PHOTOGRAPH



A) CROSS SECTION



B) SCHEMATIC

FIGURE D4. MEMORY CELL STRUCTURE

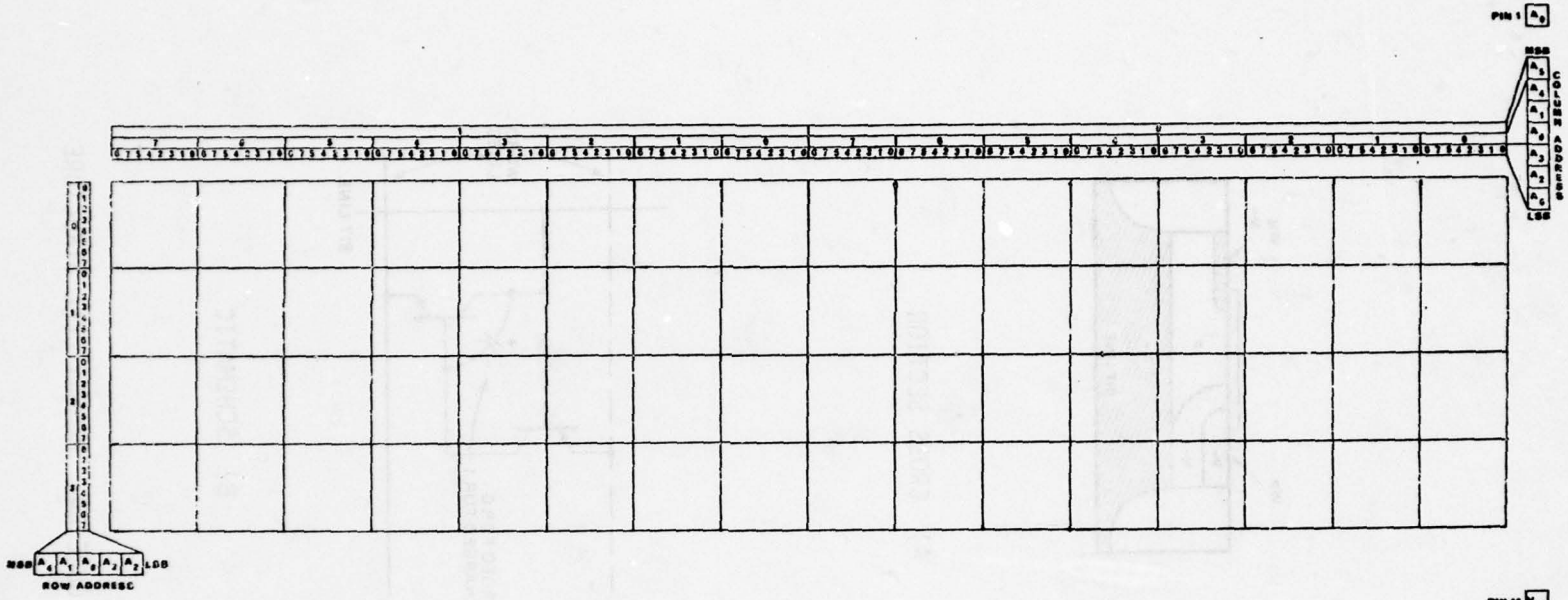
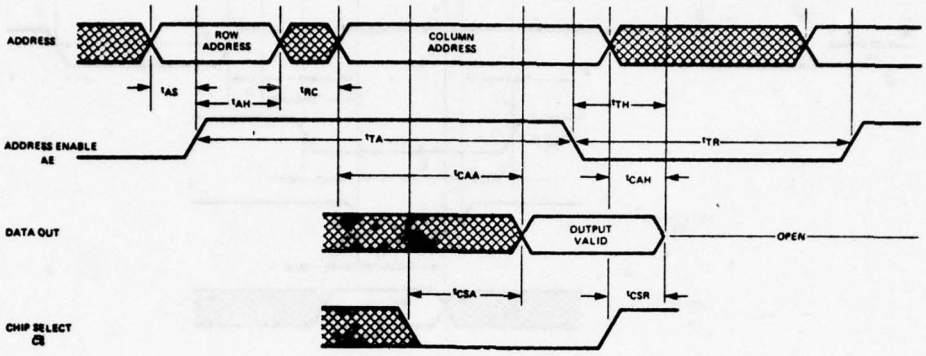


FIGURE D5. BIT MAP

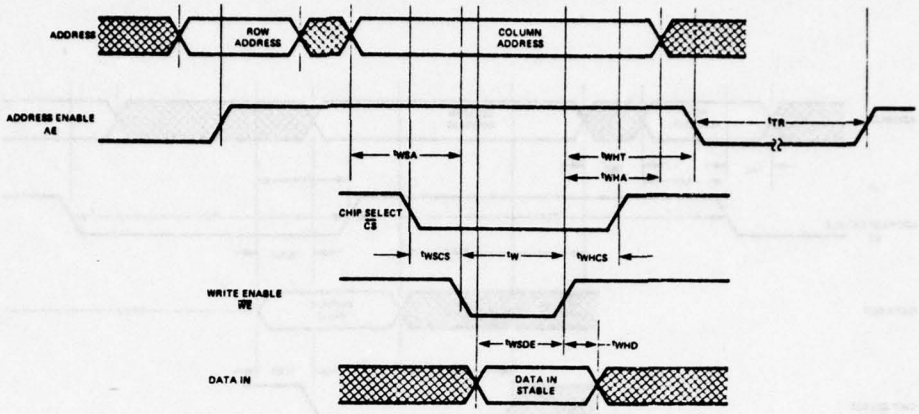


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
MULTIPLEX				
t_{AS}	Row address setup time	0		nS
t_{AH}	Row address hold time	50		
t_{TA}	AE active time	165		
t_{TR}	AE recovery time	135		nS
t_{RC}	Read cycle time	300		nS
t_{CAA}	Column address access time		100	
t_{CAH}	Output valid time after column address	10		
t_{CSA}	Chip select access time		50	
t_{CSR}	Chip select recovery time	20		
t_{TH}	Output valid time after AE	5		nS

b) TIMING TEST CONDITIONS

FIGURE D6. READ CYCLE TIMING DIAGRAM AND TEST CONDITIONS

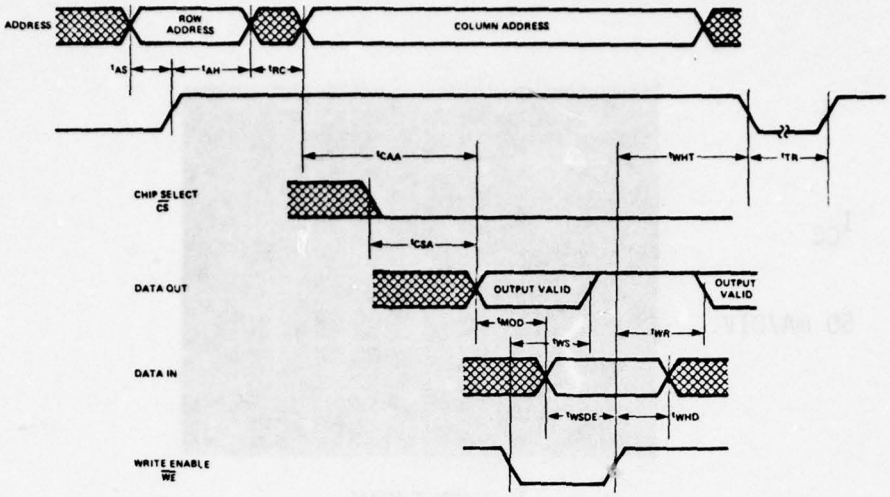


a) TIMING DIAGRAM

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
MULTIPLEX				
t_{AS}	Row address setup time	0		nS
t_{AH}	Row address hold time	50		
t_{TA}	AE active time	165		
t_{TR}	AE recovery time	135		nS
t_{WC}	Write cycle time	300		nS
t_{W}	Write pulse width	40		
t_{WSA}	Address setup time	30		
t_{WHA}	Address hold time	-5		
t_{WSCS}	Chip select setup time	10		
t_{WHCS}	Chip select hold time	0		
t_{WHT}	AE hold time after $\overline{WE}$	50		
t_{WSDE}	Data in setup time before end of $\overline{WE}$	50		
t_{WHD}	Data in hold time after $\overline{WE}$	20		nS

b) TIMING TEST CONDITIONS

FIGURE D7. WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS



a) TIMING DIAGRAM

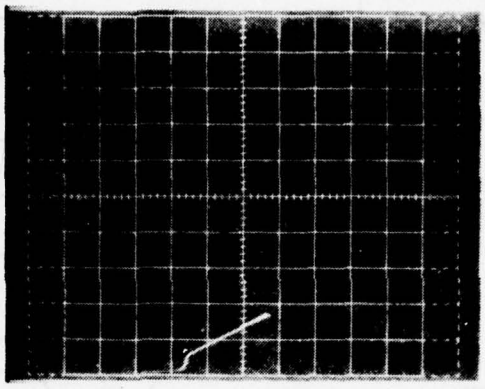
SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
MULTIPLEX				
t_{AS}	Row address setup time	0		nS
t_{AH}	Row address hold time	50		
t_{TA}	AE active time	165		
t_{TR}	AE recovery time	135		nS
t_{RMWC}	Read/modify/write cycle time	415		nS
t_{CAA}	*Column address access time*		100	
t_{CSA}	Chip select access time		50	
t_{W}	Write pulse width	40		
t_{WHT}	AE hold time after $\overline{WE}$	60		
t_{WSDE}	Data in setup time before end of $\overline{WE}$	50		
t_{WHD}	Data in hold time after $\overline{WE}$	20		
t_{WS}	Output disable time after $\overline{WE}$	35		
t_{WR}	Output recovery time after $\overline{WE}$	40		
t_{RC}	Row column address change time	20		
t_{MOD}	Data modify time	0		
$t_{/REF}$	Refresh time		2	nS

b) TIMING TEST CONDITIONS

FIGURE D8. READ/MODIFY/WRITE TIMING DIAGRAM AND TEST CONDITIONS

I_{CC}

50 mA/DIV.



V_{CC} - 1.0 VOLT/DIV.

$I_{CC} \approx 70$ mA AT V_{CC} = 5V

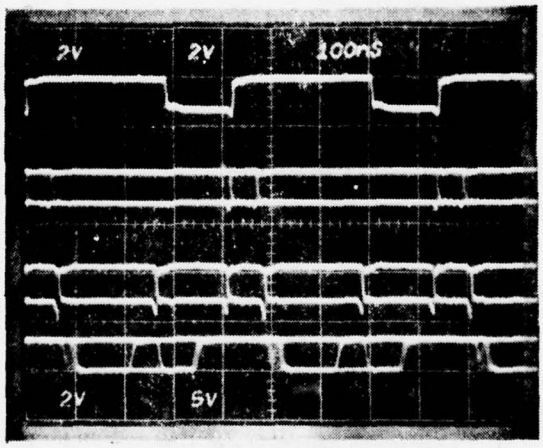
FIGURE D9. TYPICAL I_{CC} CURRENT FROM V_{CC} SUPPLY

AE

ADD

DI

DO



$t_{CAA} \approx 60$ nS AT V_{CC} = 4.75 VOLTS

FIGURE D10. TIMING WAVEFORMS FOR COLUMN ADDRESS ACCESS TIME (t_{CAA})

TABLE D1. SYMBOLS AND DEFINITIONS

SYMBOLS	DEFINITIONS
V_{CC}	SUPPLY VOLTAGE
GND	GROUND
Ao THRU A6	ADDRESS INPUT
$\overline{CS}$	CHIP SELECT INPUT
LE	LATCH ENABLE INPUT
AE	ADDRESS ENABLE INPUT
$\overline{WE}$	WRITE ENABLE INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{OH}	HIGH LEVEL OUTPUT VOLTAGE
V_{OL}	LOW LEVEL OUTPUT VOLTAGE
$V_{IC(NEG)}$	INPUT CLAMP VOLTAGE
V_{TH1}	THRESHOLD VOLTAGE
V_{THO}	THRESHOLD VOLTAGE
I_{IH}	HIGH LEVEL INPUT CURRENT
I_{IL}	LOW LEVEL INPUT CURRENT
I_{OHZ}	HIGH IMPEDANCE STATE, HIGH LEVEL OUTPUT CURRENT
I_{OLZ}	HIGH IMPEDANCE STATE, LOW LEVEL OUTPUT CURRENT
I_{CC}	SUPPLY CURRENT FROM V_{CC} SUPPLY
t_{CAA}	COLUMN ADDRESS ACCESS TIME
t_W	WRITE PULSE WIDTH
t_{AS}	ROW ADDRESS SET UP TIME
t_{AH}	ROW ADDRESS HOLD TIME
t_{WSDE}	DATA-IN SET UP TIME
t_{WHD}	DATA-IN HOLD TIME
t_{REF}	REFRESH TIME

TABLE D2. ALGORITHMS AND DESCRIPTIONS

ALGORITHM	DESCRIPTION
GALPAT	A. Write a background pattern of "0s" throughout memory. B. Write a "1" (test bit) at the first location. C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read in sequence until every location is read with test bit location. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell is used as test bit location. F. Repeat steps B through E with a background pattern of "1s" throughout memory.
GALWRT	A. Write a background pattern of "0s" throughout memory. B. Write a "1" into the background cell and read a "0" from the test bit cell. C. Repeat the sequence with the same test bit cell but the next background cell. Continue until entire memory is sequenced. D. Move test bit to next location and start sequence again. E. Repeat sequence until each cell is used as test bit location. F. Repeat steps B through E with a background pattern of "1s" throughout memory.
WALKING	A. Write a background pattern of "0s" throughout memory. B. Write a "1" at the first cell (test bit). C. Read the entire memory. D. Complement the "1" at the first cell and write a "1" into cell 2 (new test bit). E. Read the entire memory. F. Repeat the sequence until each cell is used as test bit location. G. Repeat steps B through F with a background pattern of "1s" throughout memory.
ROWPAT	A. Write a background pattern of "0s" for the first row. B. Write a "1" at the first location (test bit). C. Read location in sequence: read location 2, read test bit, read location 3, read test bit. Read until all 128 locations in row is checked with the test bit. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell in the first row is used as test bit location. F. Increment until all rows are completed. G. Repeat steps B through F with a background pattern of "1s" throughout memory.

TABLE D2. ALGORITHMS AND DESCRIPTIONS (CONT.)

MARCH	A. Write a background pattern of "0s" throughout memory. B. Incrementing from address 0 to address 4095, read a "0" and write a "1" into each cell. C. Incrementing from address 4095 to address 0, read a "1" and write an "0" into each cell. D. Repeat steps B and C with a background pattern of "1s" throughout memory.
SHIFTING DIAGONAL	A. Write a background of "0s" with a diagonal stripe of "1s". B. Read the pattern incrementing the address by one each time. C. Shift the stripe right one time. D. Read out the pattern incrementing the address by one each time. E. Repeat steps B through D until the stripe has been shifted 128 times and the pattern read out each time. F. Repeat steps B through E with a background of "1s" with a diagonal stripe of "0s".
ADDCOMP	A. Write an alternate pattern of "0s" and "1s" throughout memory. B. Verify each location by the address sequence: address, address complement, address, address + 1, etc. C. Read out data pattern from memory.
REFRESH	A. Write data (Alternating field of 1's and 0's) throughout memory. B. Pause for the maximum specified refresh time. C. Read out the pattern. D. Write the complement pattern throughout memory. E. Pause for the maximum specified refresh time. F. Read out the complement pattern.

APPENDIX E

P/N CCD450

9216 BIT DYNAMIC SHIFT REGISTER MEMORY

APPENDIX E

This appendix is included to supply various details of the Fairchild CCD450. Figures E1 and E2 are the terminal layout and the functional block diagram of the device, respectively. The Figure E3 die photograph and the bit map shown in Figure E4 provide even greater layout and function detail. The timing requirements for the read, write, and read/modify/write cycles are provided in Figures E5, E6, and E7, respectively. Further electrical characteristics are shown in the Figure E8 photograph of several waveforms during a read access time cycle.

In addition, two tables have been included in this appendix to supplement the discussion of this device in the report. Table E1 provides a list of the symbols and their definitions that are applicable to this device. Table E2 lists the algorithms used in this study of the CCD450.

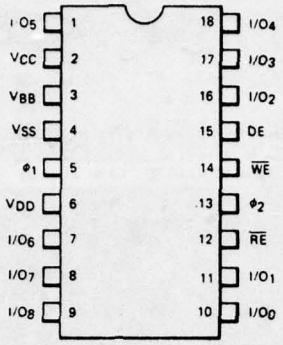


FIGURE E1. TERMINAL CONNECTION

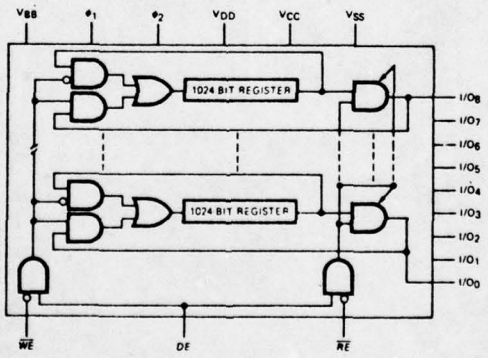


FIGURE E2. FUNCTIONAL BLOCK DIAGRAM

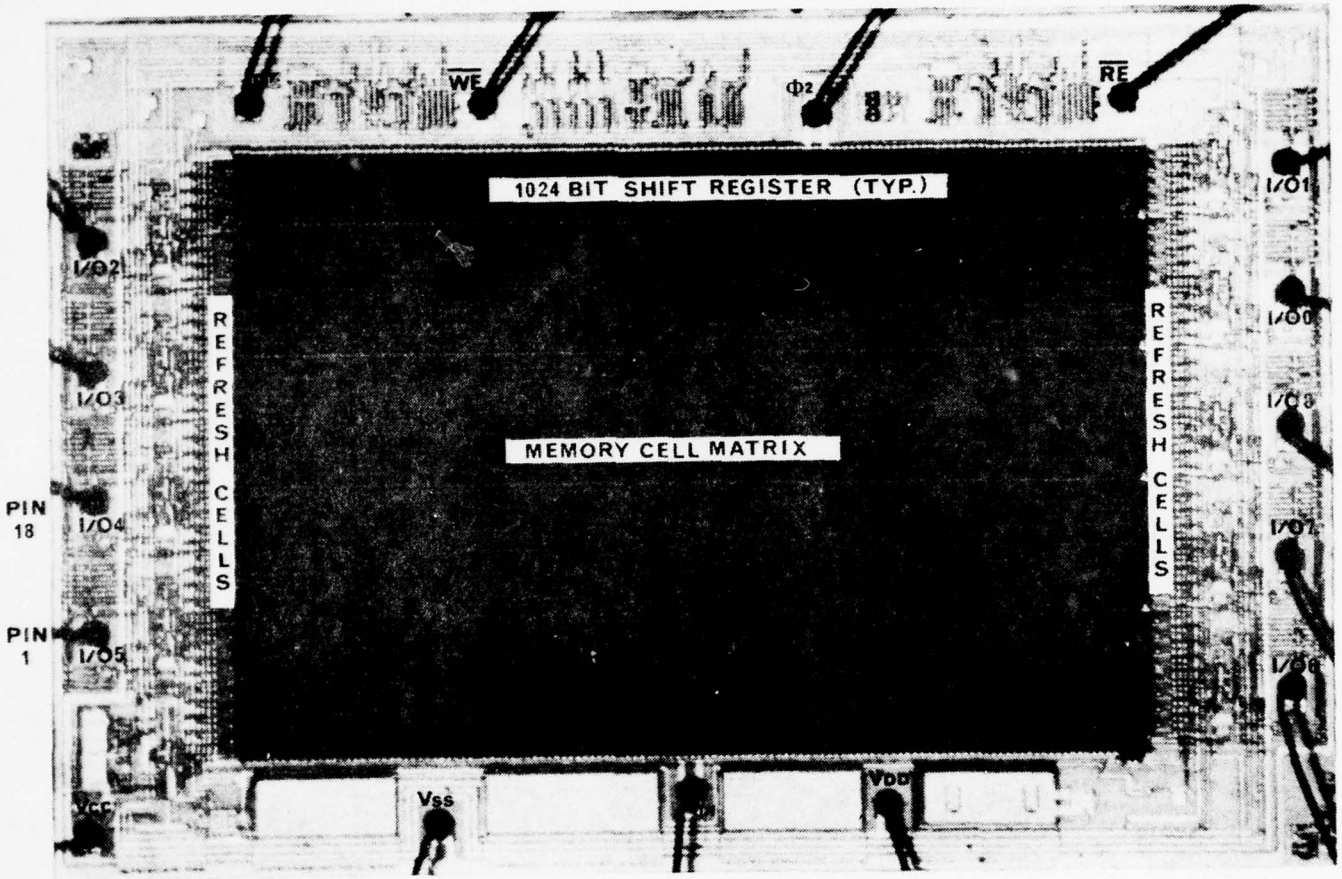
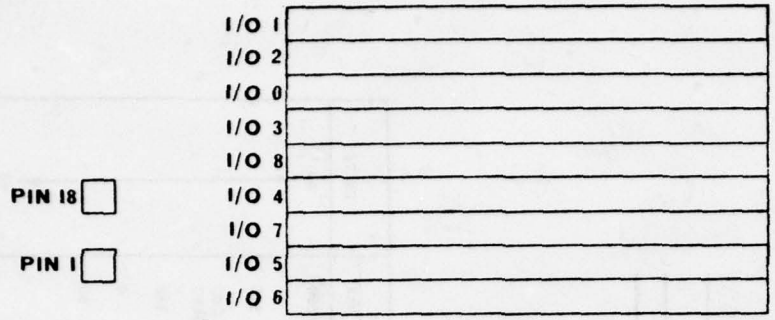


FIGURE E3. DIE PHOTOGRAPH



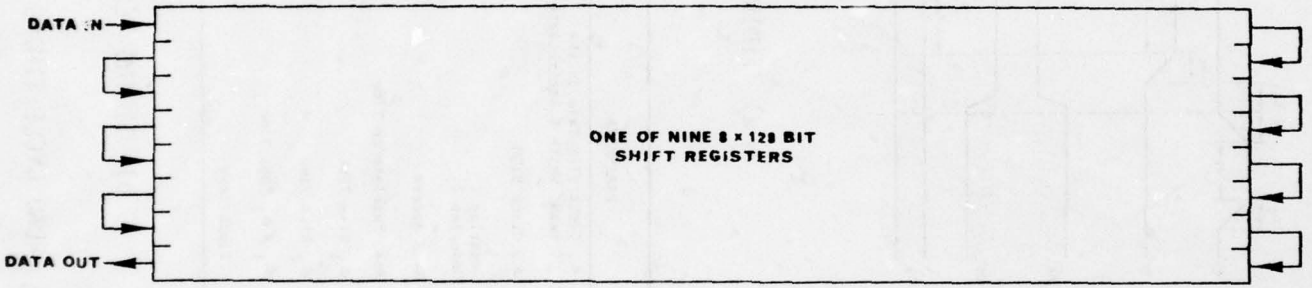


FIGURE E4. BIT MAP

AD-A079 627 MCDONNELL DOUGLAS ASTRONAUTICS CO ST LOUIS MO F/G 9/2
RELIABILITY EVALUATION AND ELECTRICAL CHARACTERIZATION OF MEMOR--ETC(U)
SEP 79 A T SASAKI F30602-77-C-0003
UNCLASSIFIED RADC-TR-79-193 NL

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AD A 079627

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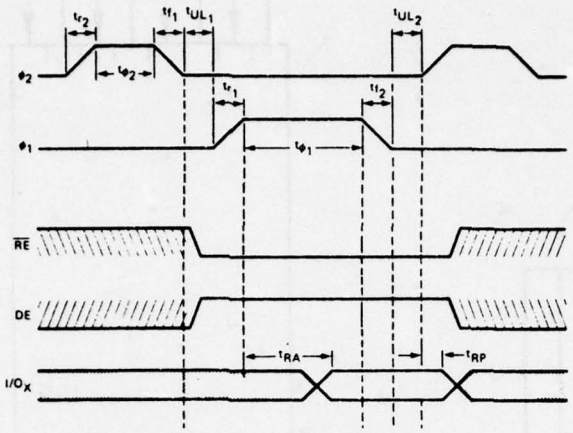
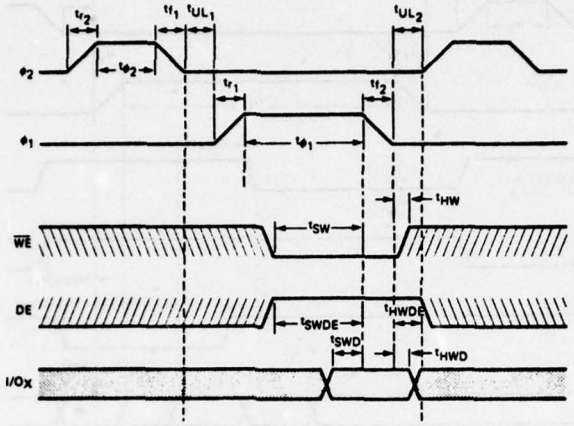


a) TIMING DIAGRAM

SYMBOL	PARAMETER	CCD450 MIN	CCD450 MAX	UNITS
$t_{\phi 1RWC}$	ϕ_1 Clock HIGH Time in the Read, Write & Recirculate Modes	200	500	nS
$t_{\phi 2}$	ϕ_2 Clock HIGH	100	500	
t_{UL} t_{UL1}	Underlap 1	20	200	
t_{UL2}	Underlap 2	20	9480	
t_{RA}	Read Access		180	
t_{RP}	Read Persistence Time		0	
t_{r1}	ϕ_1 Rise Time	50	60	
t_{r2}	ϕ_2 Rise Time	50		
t_f	ϕ_1 & ϕ_2 Fall Time	50		nS
f	Clock Rate	0.1	1.0	MHz

b) TIMING TEST CONDITIONS

FIGURE E5. READ CYCLE TIMING DIAGRAM AND TEST CONDITIONS

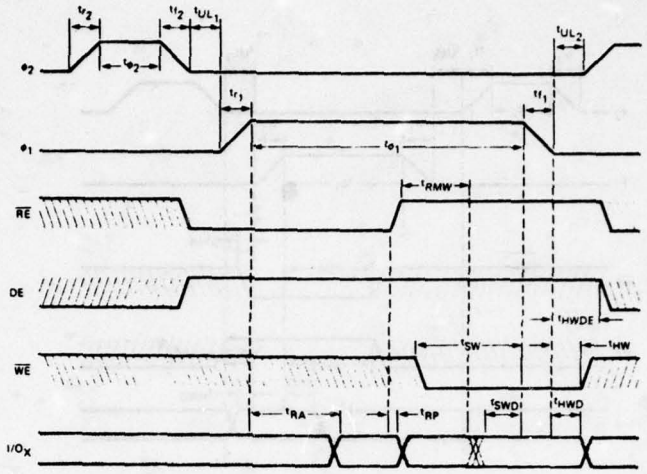


a) TIMING DIAGRAM

SYMBOL	PARAMETER	CCD450 MIN	CCD450 MAX	UNITS
$t_{\phi 1RWC}$	ϕ_1 *Clock HIGH Time in the Read, Write and Recirculate Modes*	200	500	nS
$t_{\phi 2}$	ϕ_2 Clock HIGH	100	500	
t_{UL} t_{UL1}	Underlap 1	20	200	
t_{UL2}	Underlap 2	20	9480	
t_{SW}	Write Set-up	100		
t_{HW}	Write Hold	0		
t_{SWDE}	Write Mode Data Enable Set-Up	100		
t_{HWDE}	Write Mode Data Enable Hold	0		
t_{SWD}	Write Data Set-Up	50		
t_{HWD}	Write Data Hold	0		
t_{r1}	ϕ_1 Rise Time	50	60	
t_{r2}	ϕ_2 Rise Time	50		
t_f	ϕ_1 & ϕ_2 Fall Time	50		nS
f	Clock Rate	0.1	1.0	MHz

b) TIMING TEST CONDITIONS

FIGURE E6. WRITE CYCLE TIMING DIAGRAM AND TEST CONDITIONS

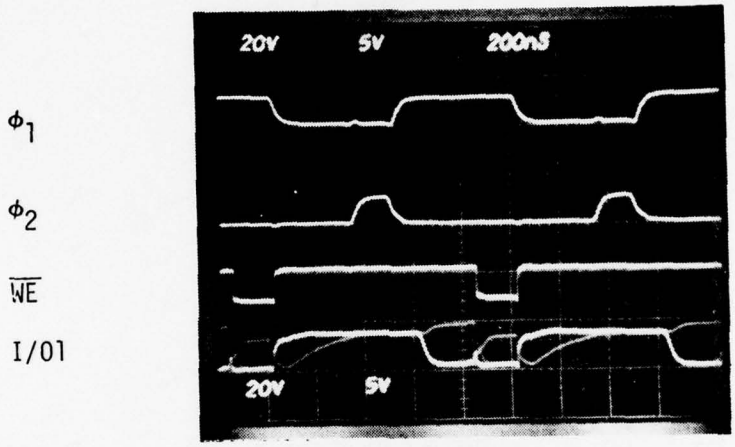


a) TIMING DIAGRAM

SYMBOL	PARAMETER	CCD450 MIN	CCD450 MAX	UNITS
$t_{\phi 1RMW}$	ϕ_1 Clock HIGH Time in the Read/Modify/Write Mode	350	500	nS
$t_{\phi 2}$	ϕ_2 Clock HIGH	100	500	
t_{UL} t_{UL1}	Underlap 1	20	200	
t_{UL} t_{UL2}	Underlap 2	20	9480	
t_{RMW}	Read Enable High Time in Read/Modify/Write Mode	50		
t_{RA}	Read Access		180	
t_{RP}	Read Persistence Time		0	
t_{SW}	Write Set-up	100		
t_{HW}	Write Hold	0		
t_{SWDE}	Write Mode Data Enable Set-up	50		
t_{HWDE}	Write Mode Data Enable Hold	0		
t_{SWD}	Write Data Set-Up	50		
t_{HWD}	Write Data Hold	0		
t_{r1}	ϕ_1 Rise Time	50	60	
t_{r2}	ϕ_2 Rise Time	50		
t_f	ϕ_1 & ϕ_2 Fall Time	50		nS
f	Clock Rate	0.1	1.0	MHz

b) TIMING TEST CONDITIONS

FIGURE E7. READ/MODIFY/WRITE TIMING DIAGRAM AND TEST CONDITIONS



$t_{RA} \approx 120$ NS AT V_{CC} = 12.0 VOLTS,
V_{BB} = -3.0 VOLTS, V_{CC} = 5.0 VOLTS

FIGURE E8. TIMING WAVEFORMS FOR TYPICAL READ ACCESS TIME (t_{RA})

TABLE E1. SYMBOLS AND DEFINITIONS

SYMBOL	DEFINITION
V_{DD}	SUPPLY VOLTAGE
V_{CC}	SUPPLY VOLTAGE
V_{BB}	SUBSTRATE VOLTAGE
V_{SS}	COMMON NODE VOLTAGE
I/O	INPUT/OUTPUT
Φ_1	CLOCK 1
Φ_2	CLOCK 2
DE	DATA ENABLE
$\overline{WE}$	WRITE ENABLE
$\overline{RE}$	READ ENABLE
V_{OH}	HIGH LEVEL OUTPUT VOLTAGE
V_{OL}	LOW LEVEL OUTPUT VOLTAGE
I_{IH}	HIGH LEVEL INPUT CURRENT
I_{DD}	SUPPLY CURRENT FROM V_{DD} SUPPLY
I_{CC}	SUPPLY CURRENT FROM V_{CC} SUPPLY
I_{BB}	SUPPLY CURRENT FROM V_{BB} SUPPLY
V_{TH1}	INPUT THRESHOLD VOLTAGE
V_{TH0}	INPUT THRESHOLD VOLTAGE
t_{RA}	READ ACCESS TIME
$t_{\Phi 2}$	CLOCK 2 HIGH TIME
t_{SW}	WRITE SETUP TIME
t_{SWD}	WRITE DATA SETUP TIME

TABLE E2. ALGORITHMS AND DESCRIPTIONS

ALGORITHM	DESCRIPTION
SCAN1	A. Write a pattern of '1s' throughout memory. B. Read '1s' from each memory location.
SCAN0	A. Write a pattern of '0s' throughout memory. B. Read '0s' from each memory location.
SHIFT REGISTER WALK (SRWALK)	A. Write a pattern of '1s' throughout memory. B. Write a '0' into Shift Register (SR) 1. C. Read, shift data 1024 times and read. D. Rewrite a '1' into starting location. E. Repeat sequence until each cell is used as test bit location. F. Repeat sequence until all 9 shift registers have been tested. G. Repeat steps B through F with pattern of '0s' throughout memory.
ALTWOR	A. Write a pattern sequence as follows into memory: 0011....0011 for all 9 shift registers. B. Read pattern from memory. C. Repeat steps A - B with complement pattern.
CHECKERBOARD1 (CBOARD1)	A. Write an alternate pattern of '1s' and '0s' in ascending bit locations of each shift register. Start with '1' in address 0.

TABLE E2. ALGORITHMS AND DESCRIPTIONS (CONT.)

CHECKERBOARD1 (CBOARD1) CONTINUED	B. Read pattern from memory. C. Repeat steps A - B by starting with '0' in address 0.
CHECKERBOARD2 (CBOARD2)	A. Write an alternate pattern of 'ls' and 'Os' in SR1 starting with '0' in address 0. B. Write an alternate pattern of 'ls' and 'Os' in SR2 starting with '1' in address 1. C. SR3, 5, 7, 9 has identical data as SR1. D. SR4, 6, 8 has identical data as SR2. E. Read pattern from memory. F. Repeat steps A - E with data complemented.

APPENDIX F

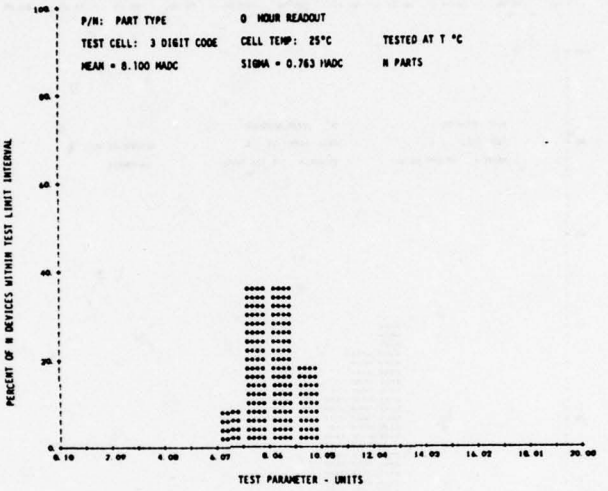
MEMORY TYPES HISTOGRAMS AND SHMOOS

TABLE OF CONTENTS

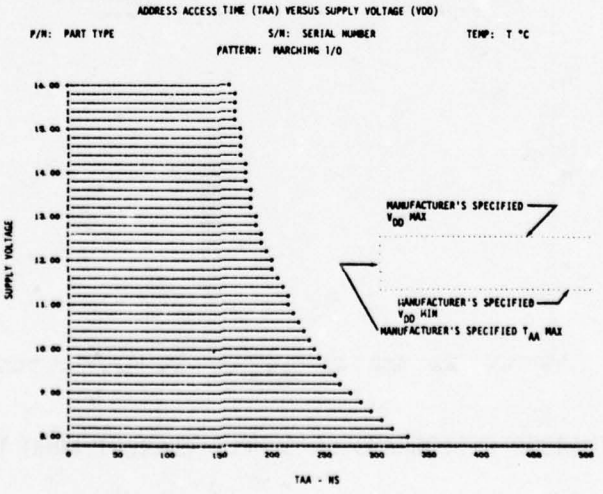
1.0 INTRODUCTION

This section contains the part types histograms and shmoos at the various test temperatures. The histogram is a graphical presentation of the frequency distribution of 100% of a parameter test data. The shmoo is a plot of the device pass and fail data as a function of two parameters, e.g., supply voltage and access time. A typical example of a histogram and shmoo is illustrated below.

SAMPLE HISTOGRAM



SAMPLE SHMOO



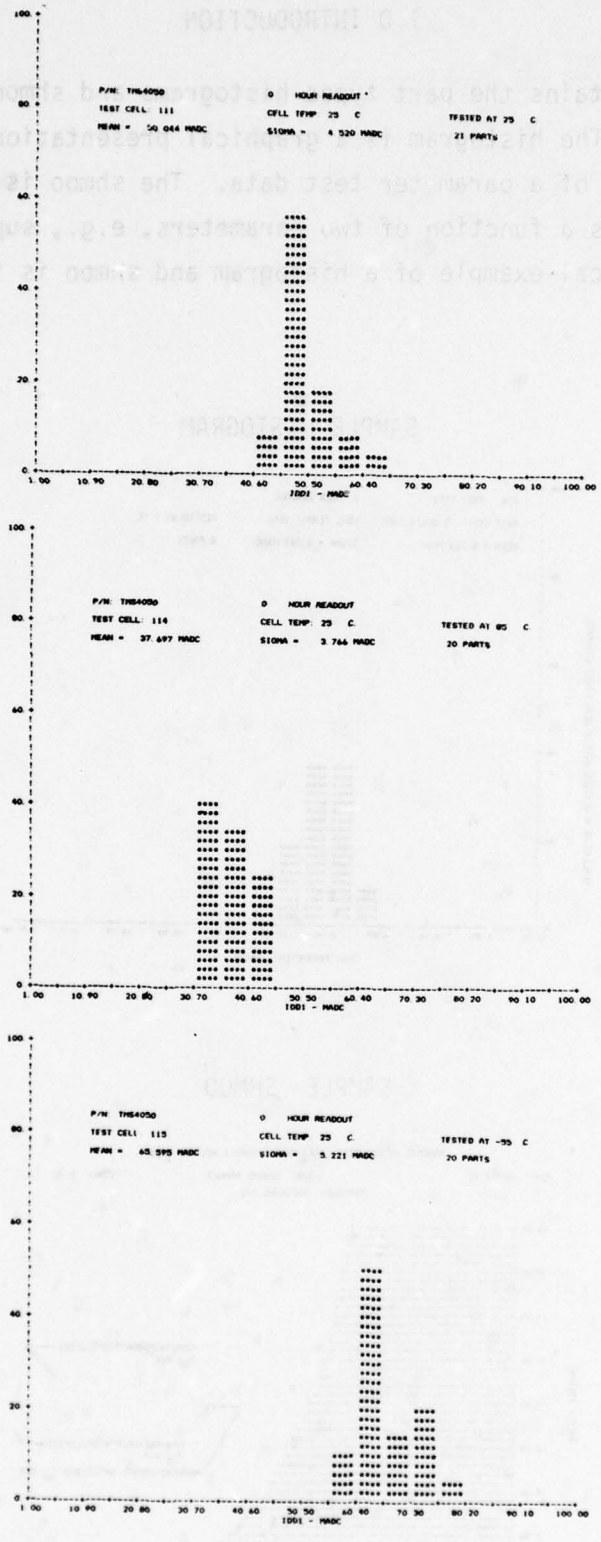


FIGURE F1. TMS4050 HISTOGRAMS OF SUPPLY CURRENT FROM THE V_{DD} SUPPLY

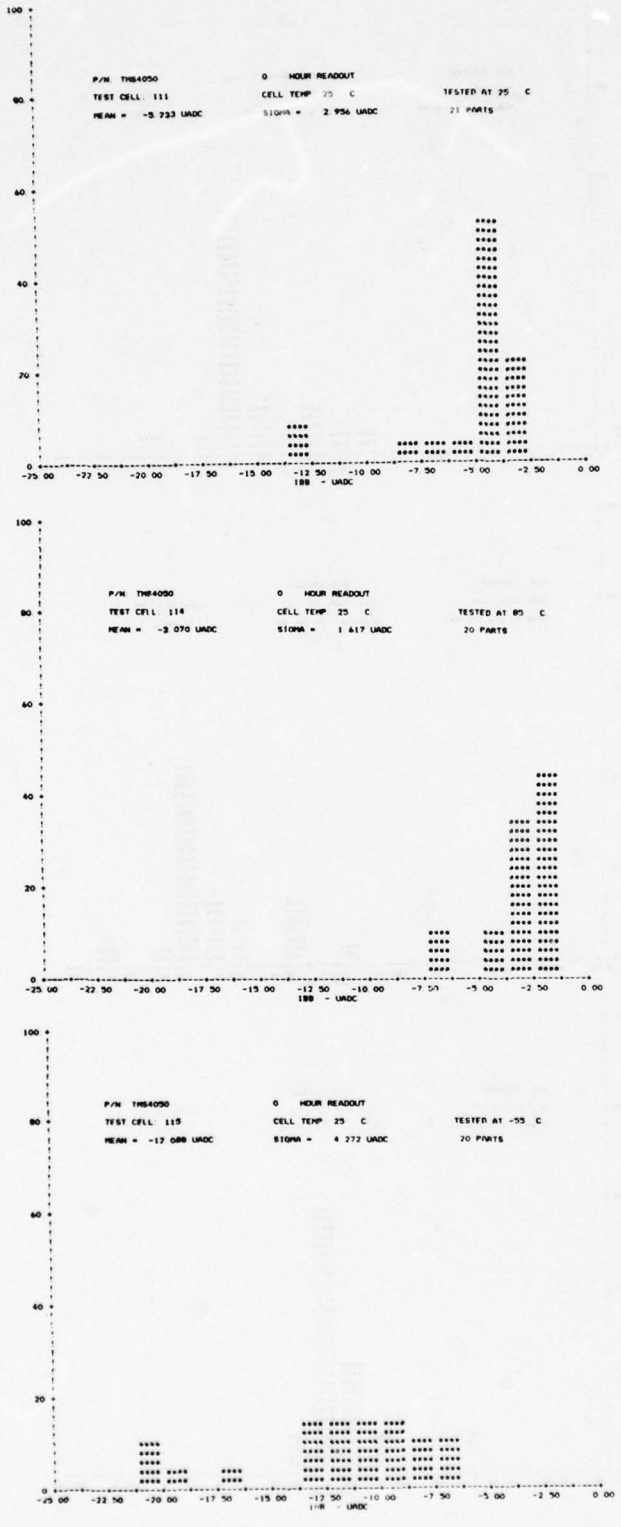


FIGURE F2. TMS4050 HISTOGRAMS OF SUPPLY CURRENT FROM V_{BB} SUPPLY

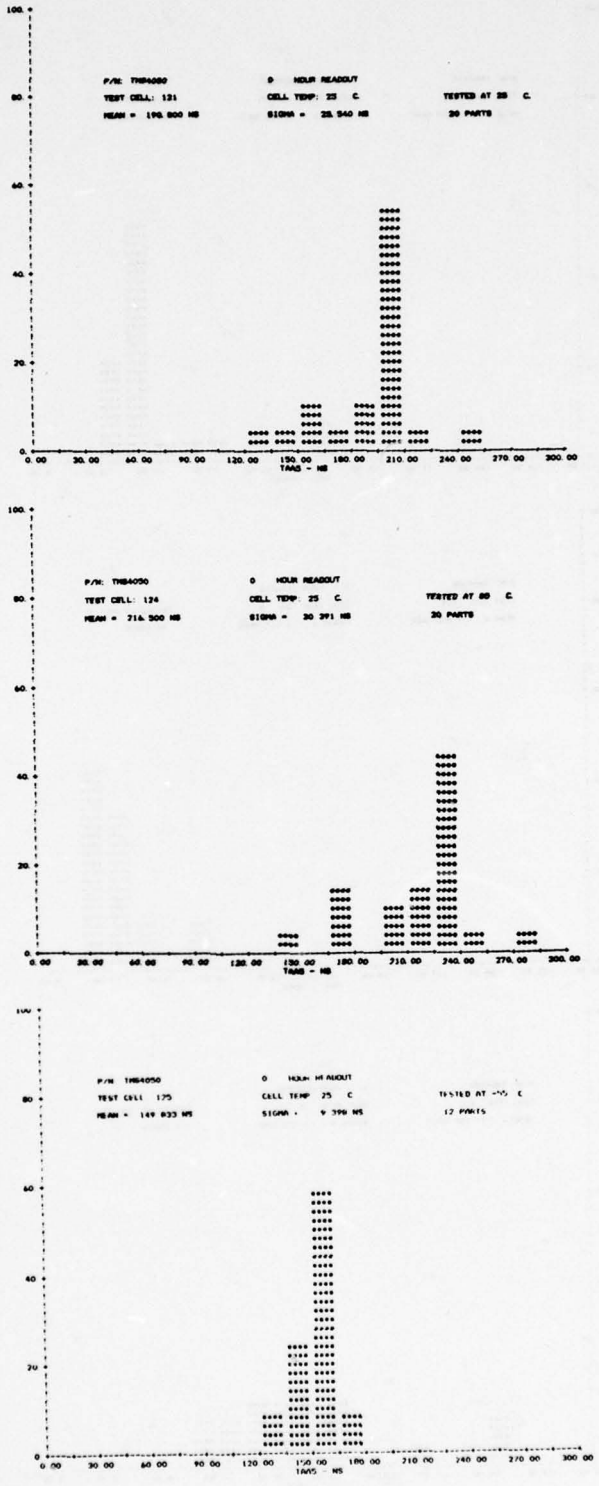
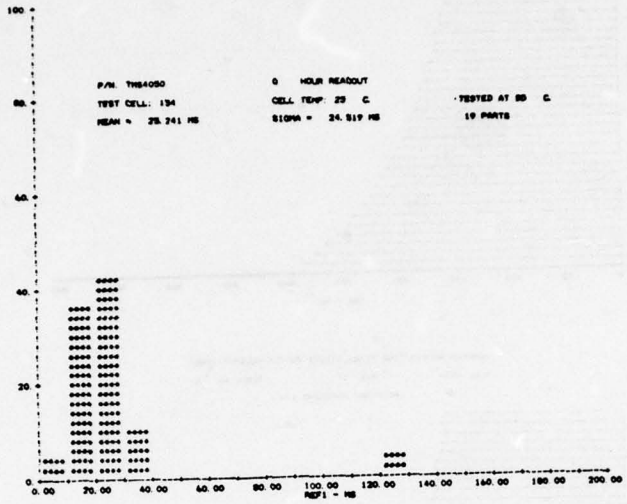


FIGURE F3. TMS4050 HISTOGRAMS OF ADDRESS ACCESS TIME - MARCHING PATTERN



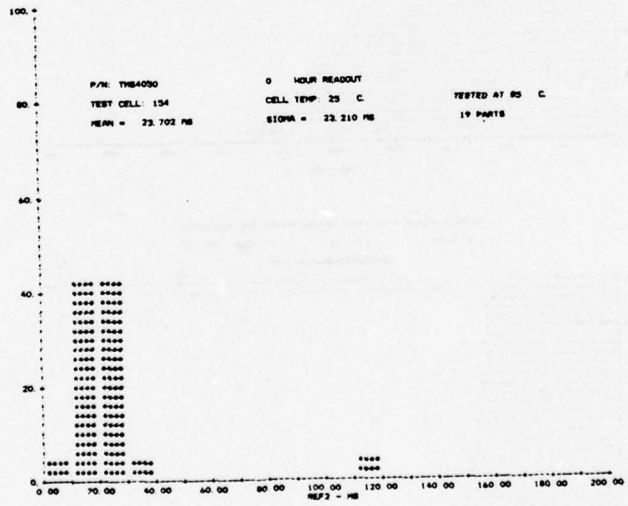


FIGURE F4. TMS4050 HISTOGRAMS OF REFRESH TIME - CHECKERBOARD PATTERN

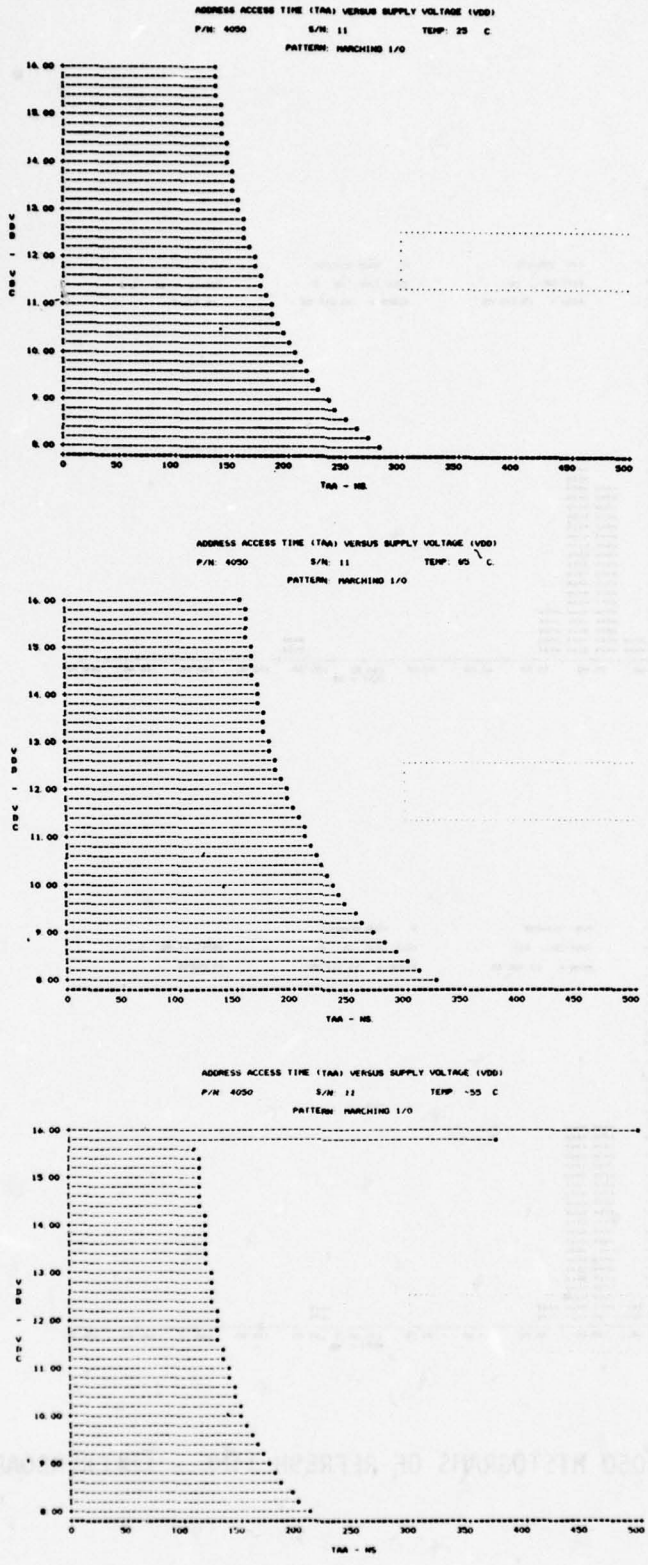


FIGURE F5. TMS4050 SHMOOS FOR ADDRESS ACCESS TIME - MARCHING PATTERN

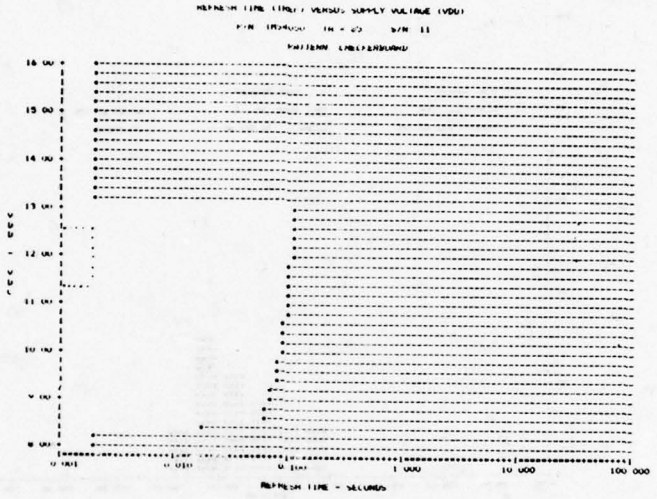


FIGURE F6. TMS4050 SHMOO FOR REFRESH TIME - CHECKERBOARD PATTERN

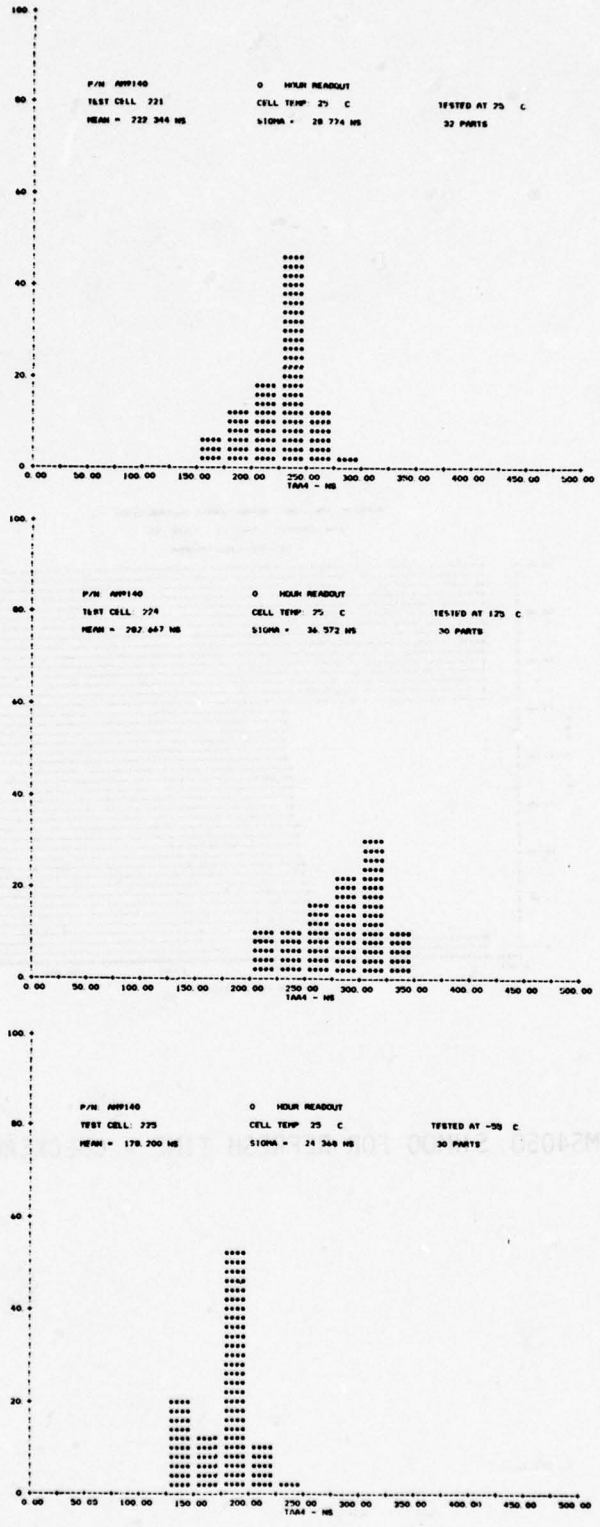


FIGURE F7. AM9140 HISTOGRAMS OF CHIP ENABLE ACCESS TIME - ROWPAT PATTERN

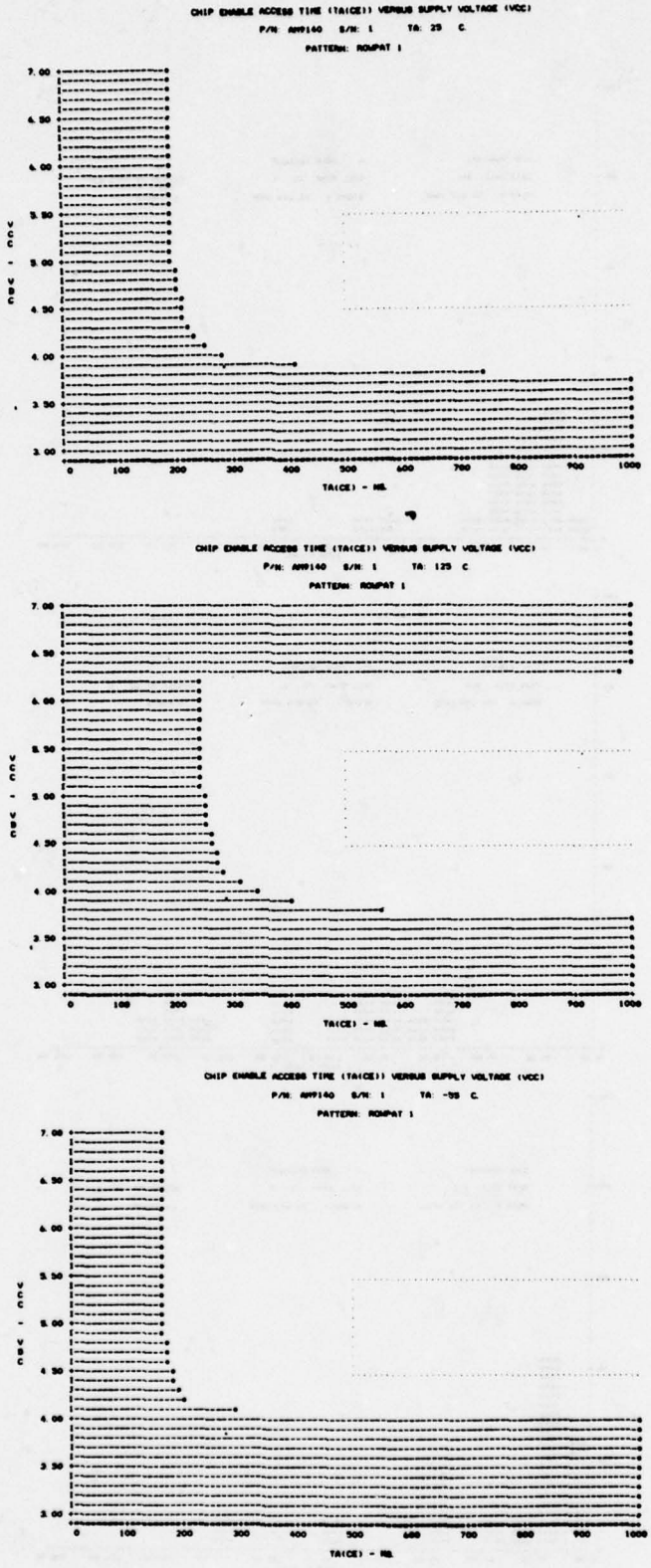


FIGURE F8. AM9140 SHMOOS FOR CHIP ENABLE ACCESS TIME - ROWPAT PATTERN

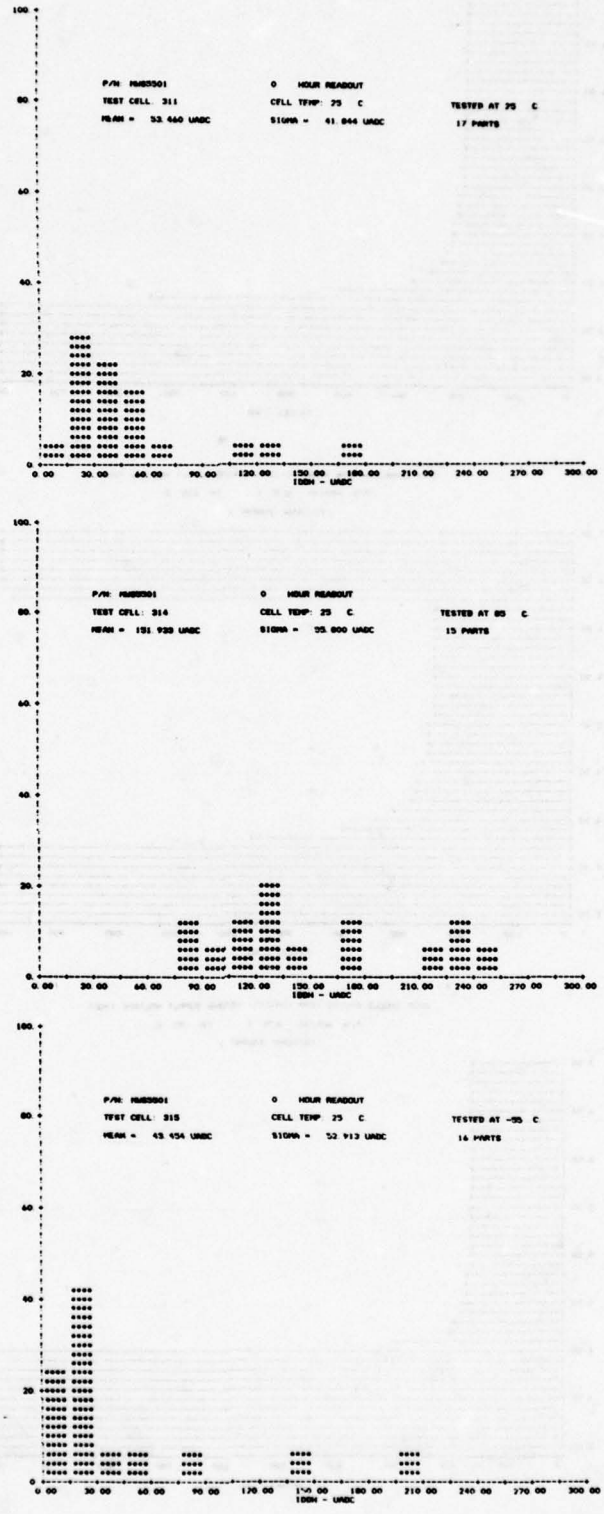


FIGURE F9. MWS5501 HISTOGRAMS OF SUPPLY CURRENT WITH V_{DD} = 10.5 VOLTS

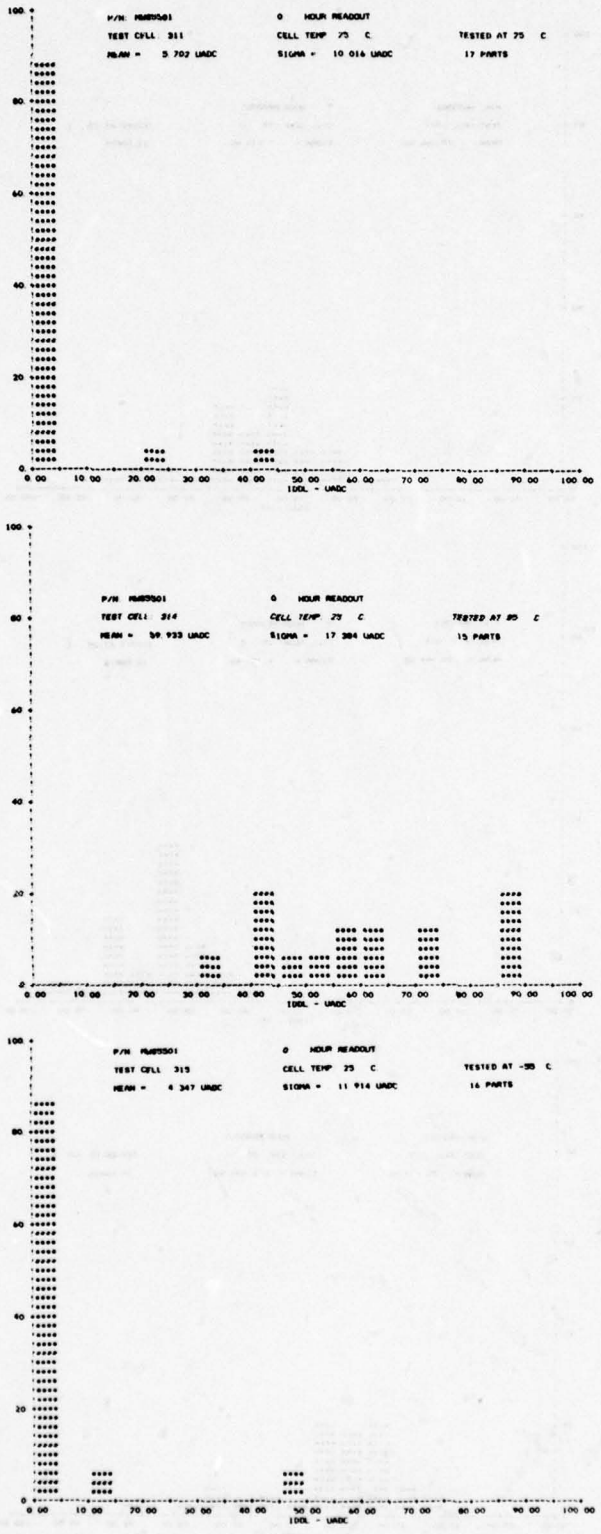


FIGURE F10. MWS5501 HISTOGRAMS OF SUPPLY CURRENT WITH V_{DD} = 5.25 VOLTS

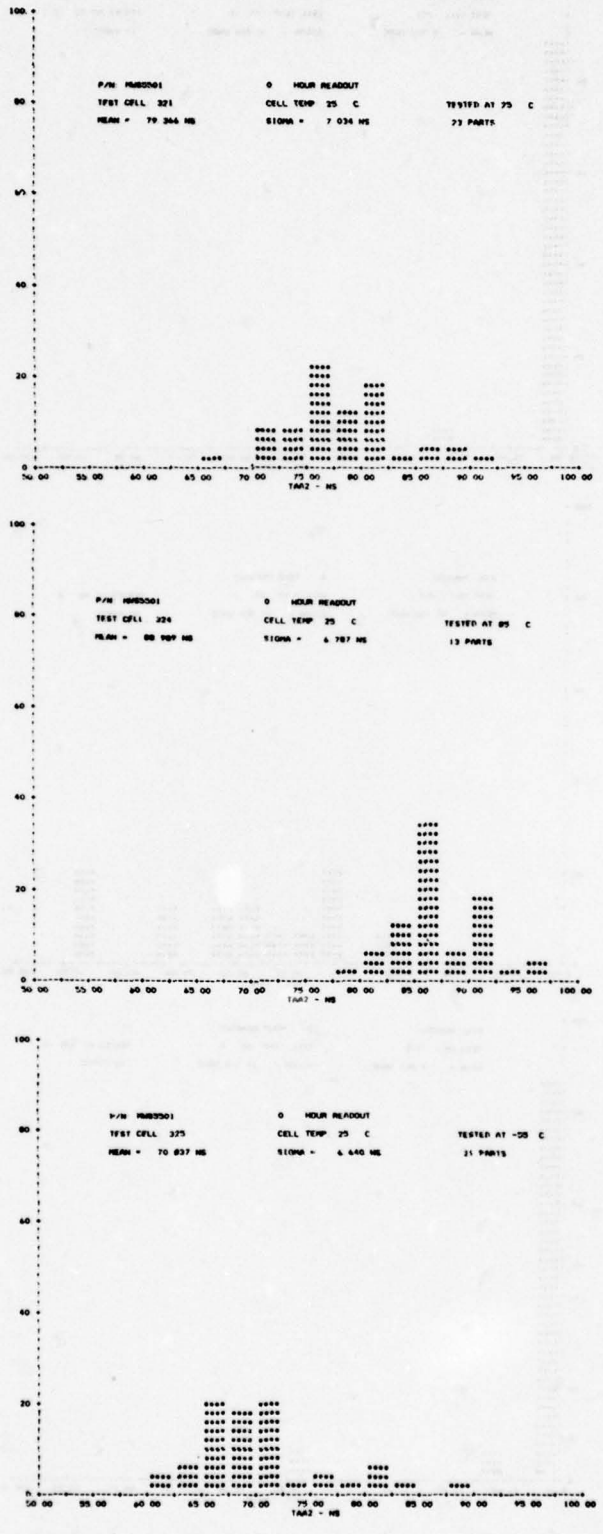


FIGURE F11. MWS5501 HISTOGRAMS OF ADDRESS ACCESS TIME - WALKING PATTERN

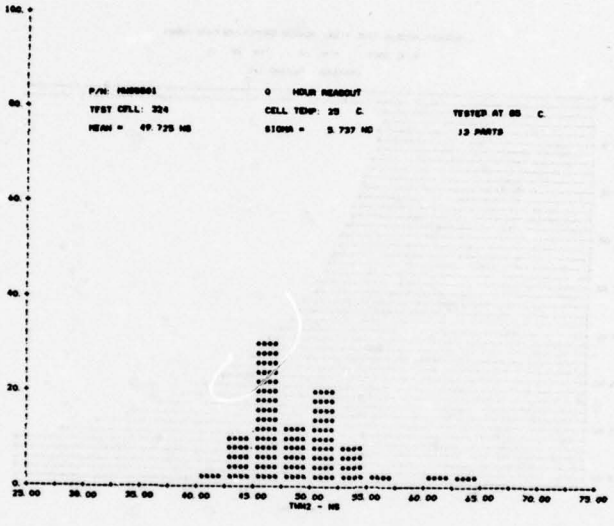


FIGURE F12. MWS5501 HISTOGRAM OF WRITE PULSE WIDTH - WALKING PATTERN

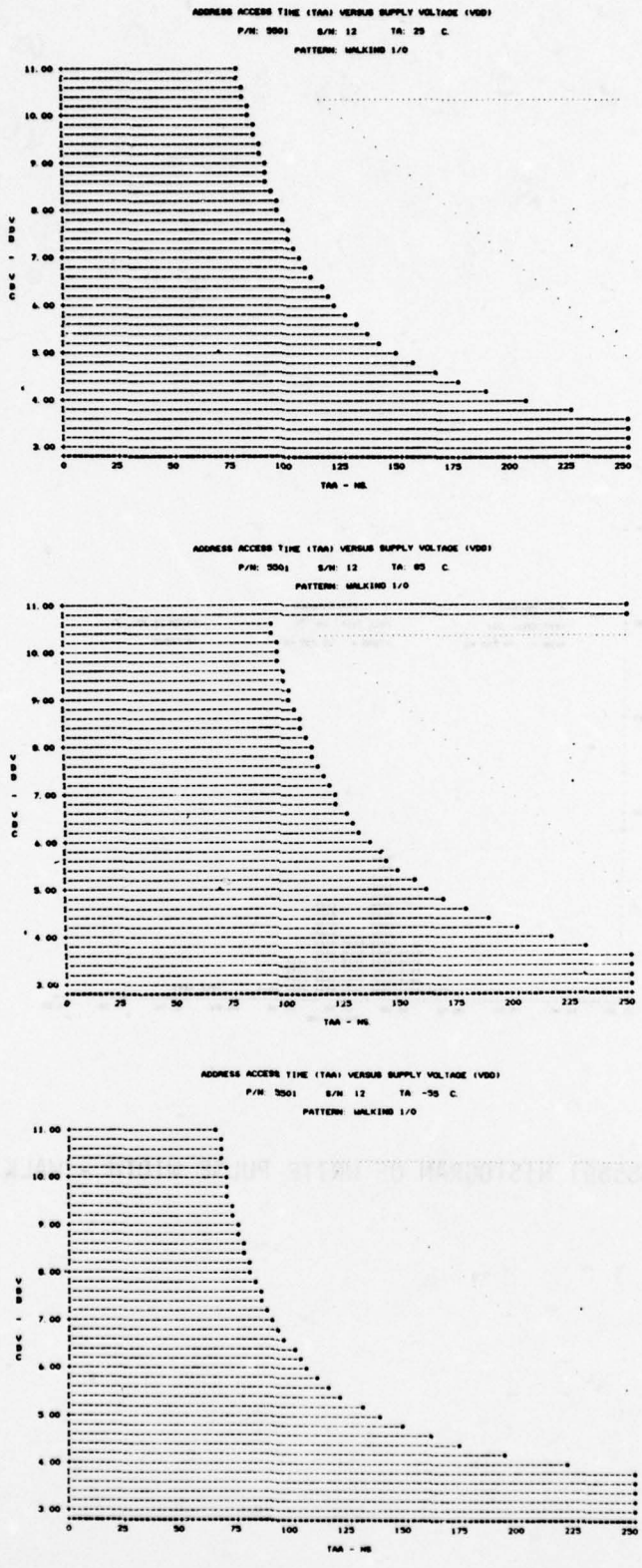


FIGURE F13. MWS5501 SHMOOS FOR ADDRESS ACCESS TIME - WALKING PATTERN

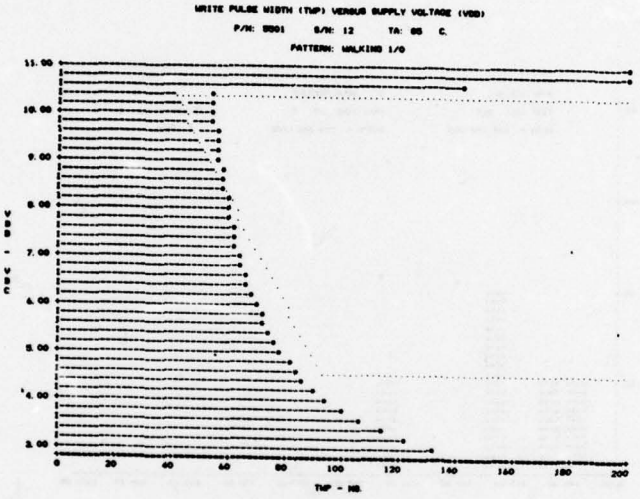


FIGURE F14. MWS5501 SHMOO FOR WRITE PULSE WIDTH - WALKING PATTERN

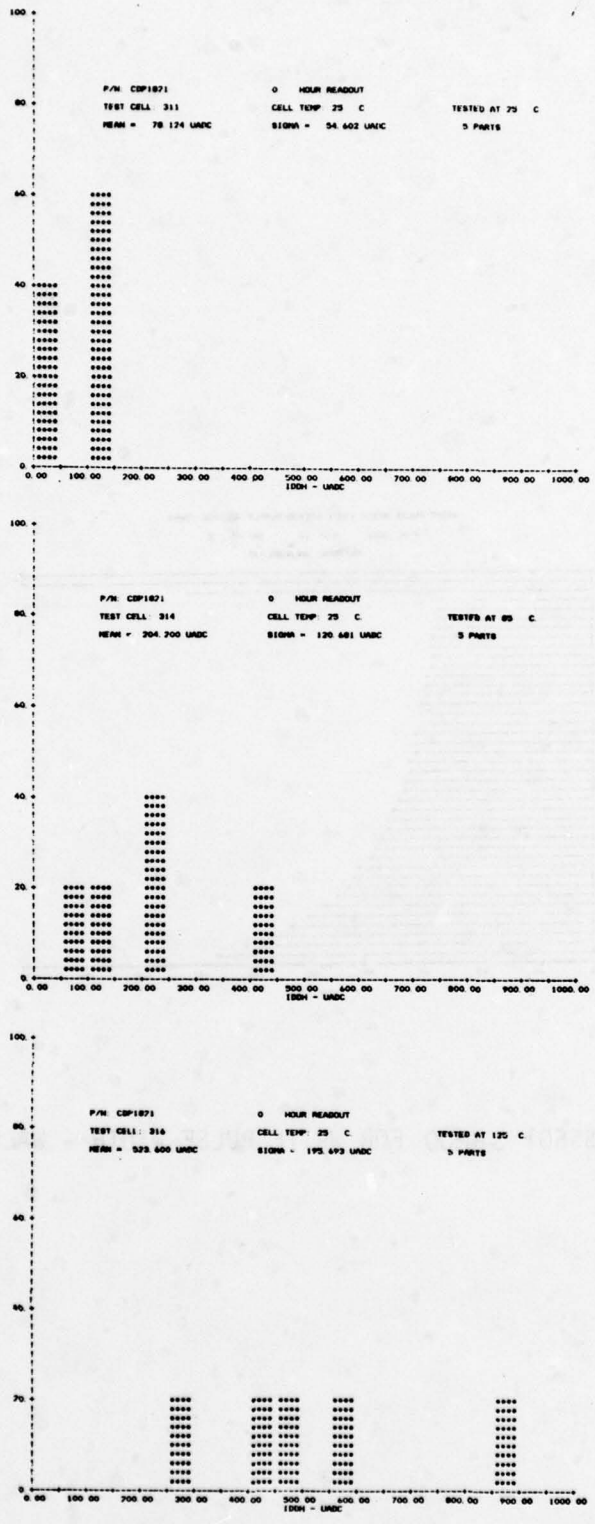


FIGURE F15. CDP1821 HISTOGRAMS OF SUPPLY CURRENT WITH V_{DD} = 10.5 VOLTS

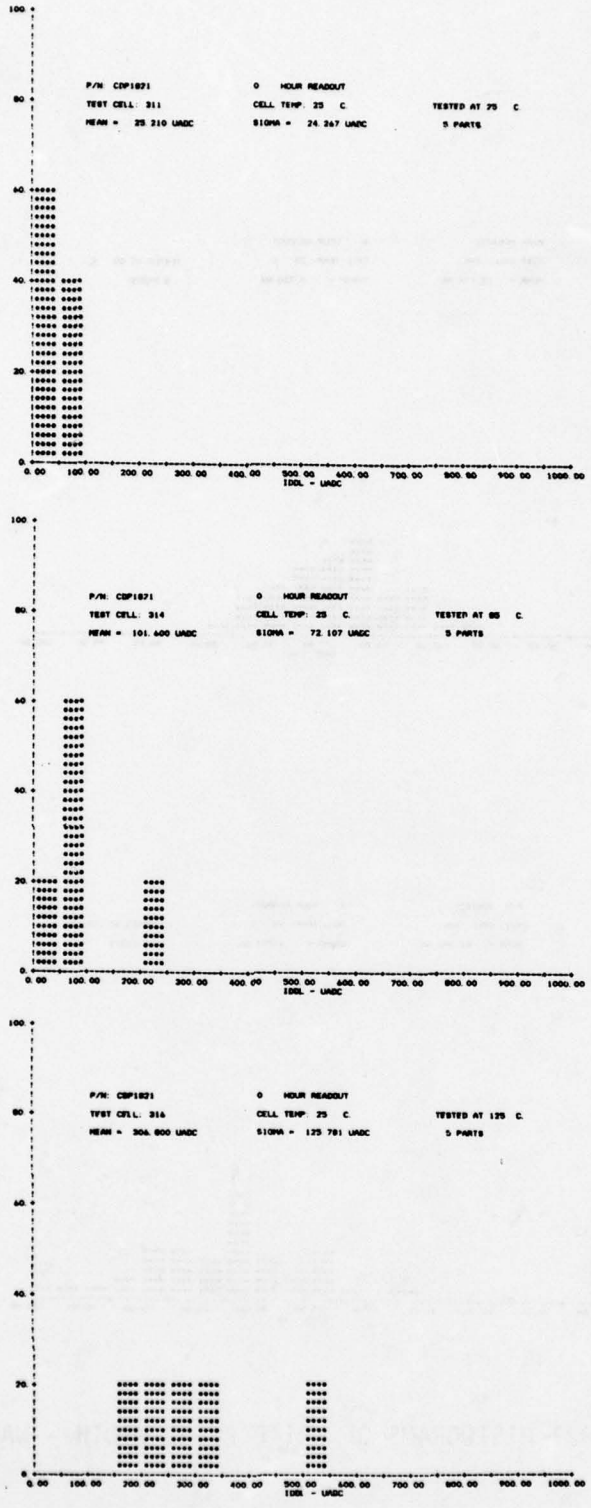
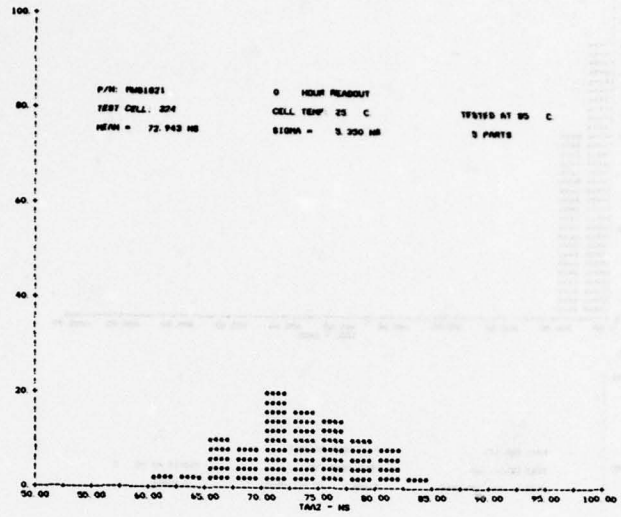


FIGURE F16. CDP1821 HISTOGRAMS OF SUPPLY CURRENT WITH V_{DD} = 5.25 VOLTS



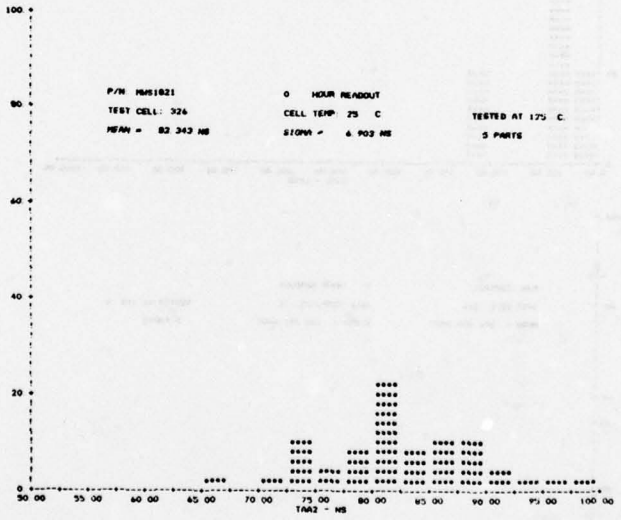
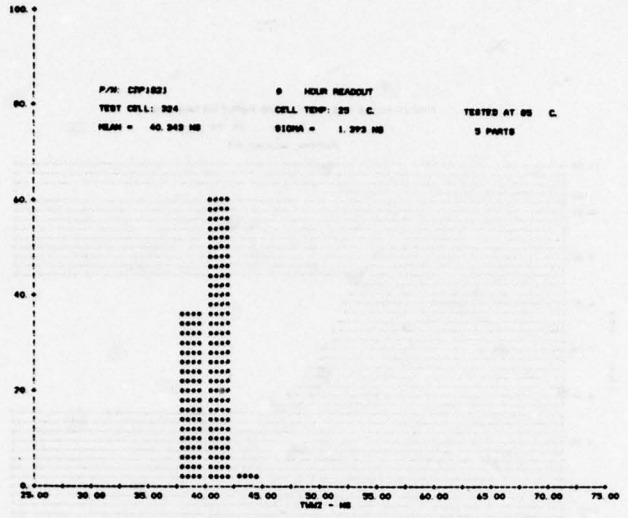


FIGURE F17. CDP1821 HISTOGRAMS OF WRITE PULSE WIDTH - WALKING PATTERN



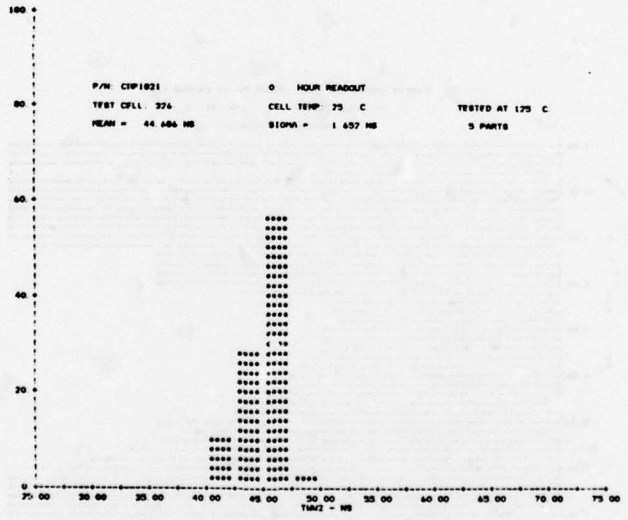
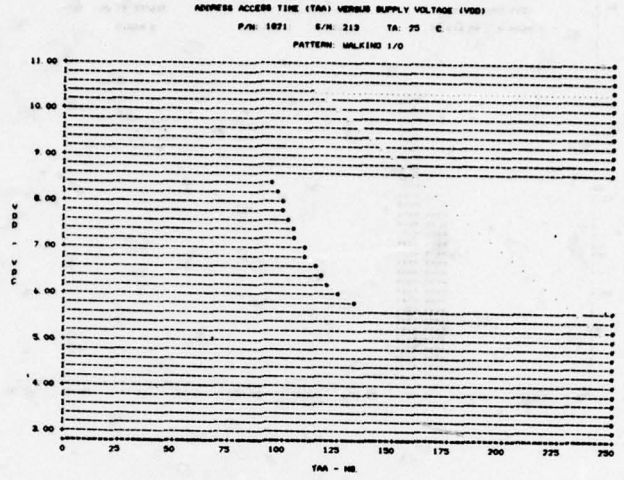


FIGURE F18. CDP1821 HISTOGRAMS OF ADDRESS ACCESS TIME - WALKING PATTERN



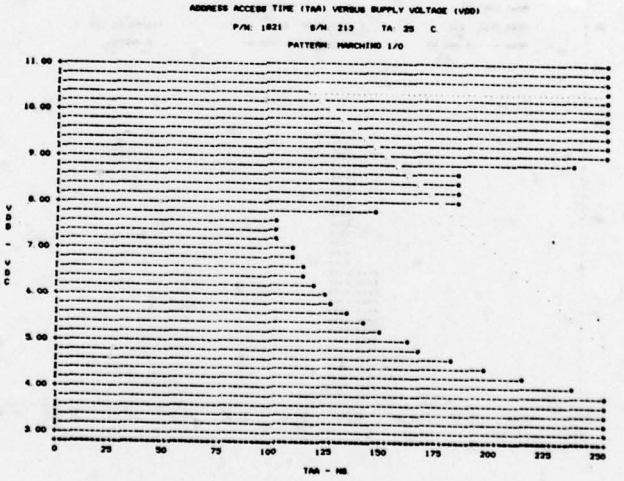
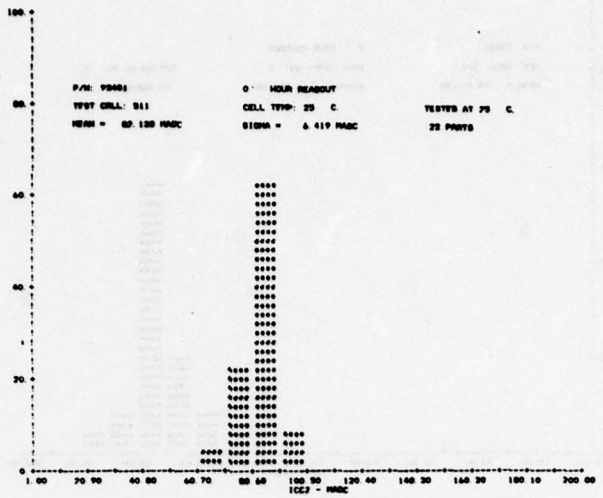
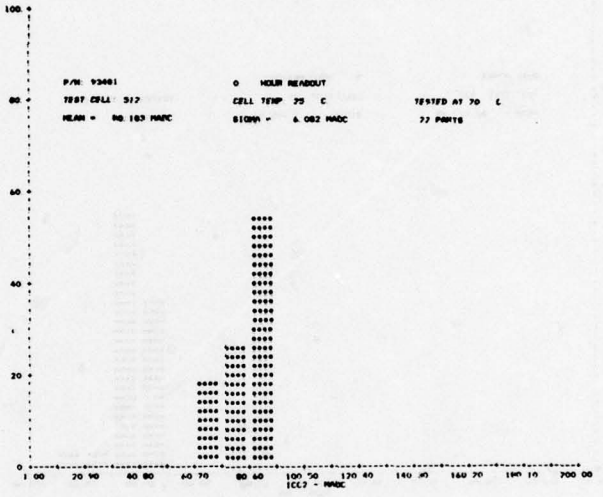


FIGURE F19. CDP1821 SHMOOS FOR ADDRESS ACCESS TIME - WALKING AND MARCHING PATTERNS





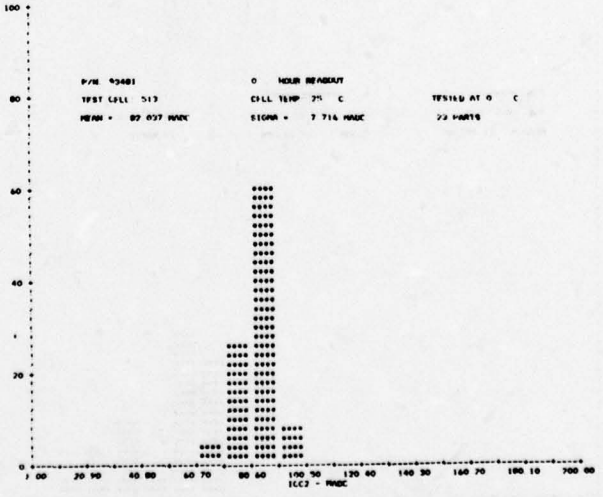


FIGURE F20. 93481 HISTOGRAMS OF SUPPLY CURRENT

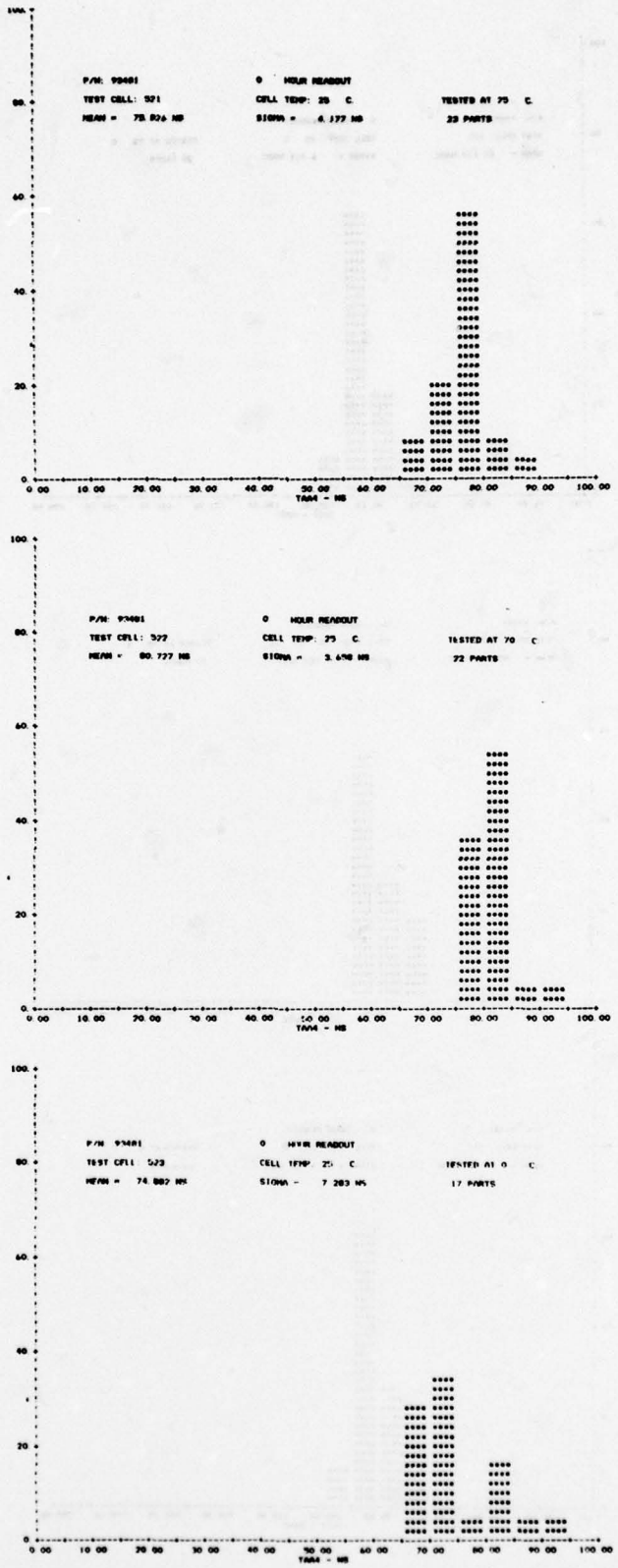
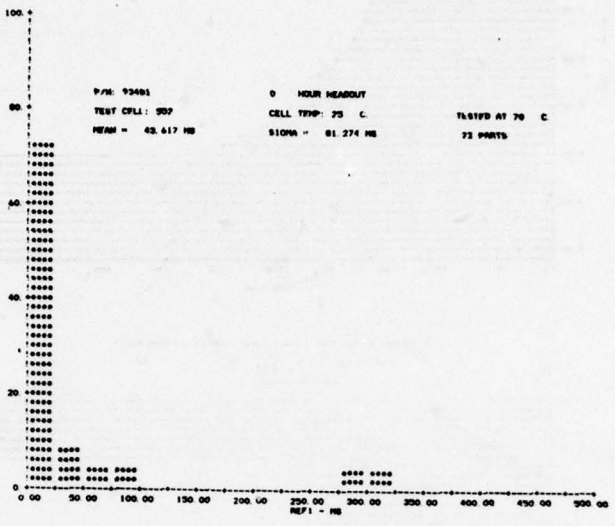


FIGURE F21. 93481 HISTOGRAMS OF COLUMN ADDRESS ACCESS TIME - ROWPAT PATTERN



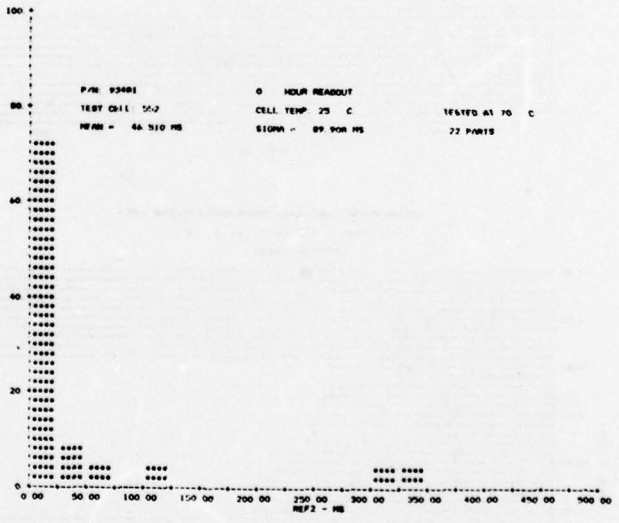
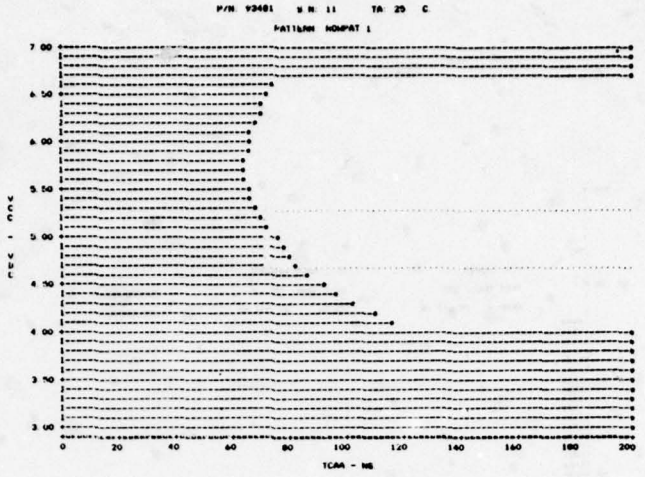
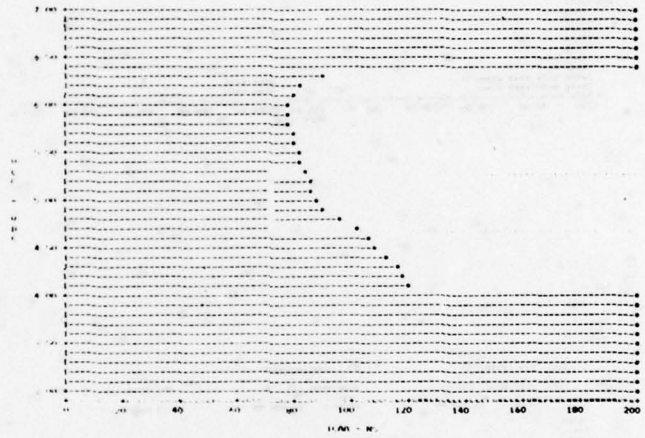


FIGURE F22. 93481 HISTOGRAMS OF REFRESH TIME - CHECKERBOARD PATTERN





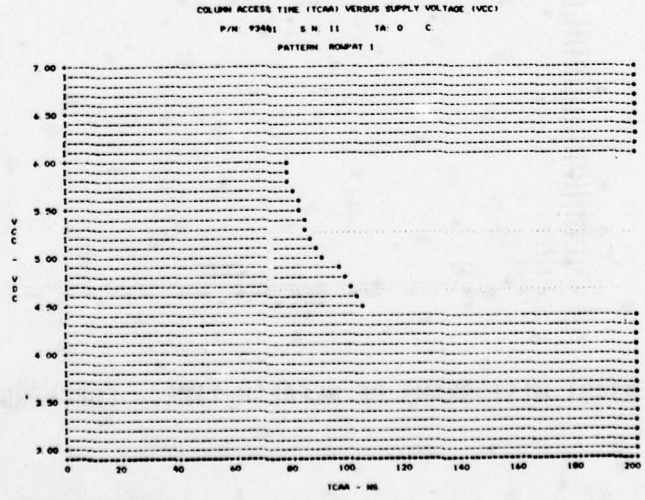


FIGURE F23. 93481 SHMOOS FOR COLUMN ADDRESS ACCESS TIME - ROWPAT PATTERN

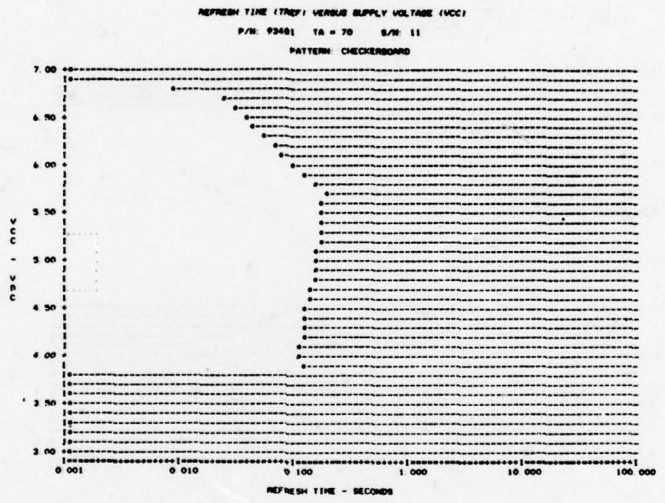


FIGURE F24. 93481 SHMOO FOR REFRESH TIME - CHECKERBOARD PATTERN

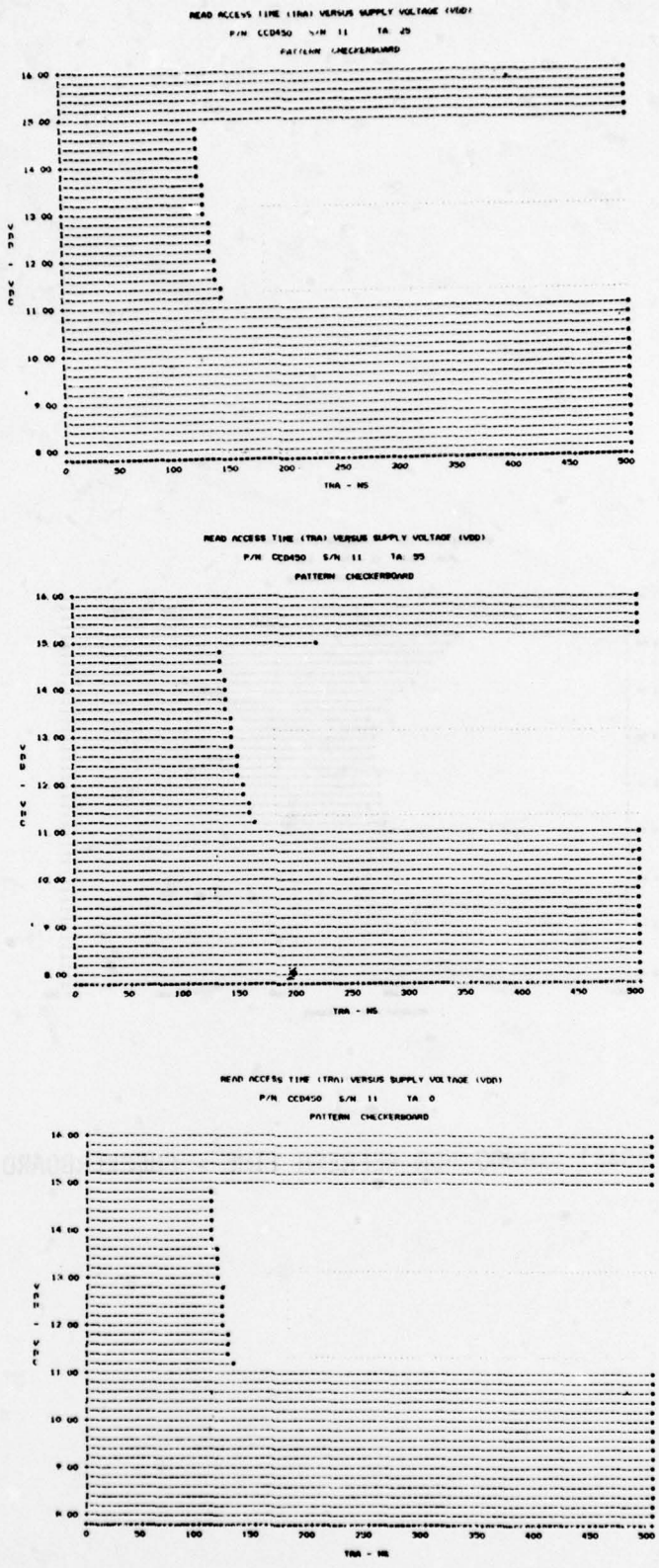


FIGURE F25. CCD450 SHMOOS FOR READ ACCESS TIME - CHECKERBOARD PATTERN

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RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.